Life as a Graduate at Cirrus Logic

Verification Perspective

Experts in Low-Power Audio and High-Performance Mixed-Signal Processing

Ben Harper, Vladislav Rumiantsev

Contents

Background – Ben

- From a golf town in Scotland
- Heriot-Watt University
- Originally doing Robotics int. MEng
- Switched to EEE in 3rd year
- Focused on programming in 4/5th
- Placement with STMicroelectronics 5th year
- Graduated into Cirrus

Background – Vlad

- **Edinburgh Uni EEE Graduate 2019**
  - Digital Design
  - Embedded C
  - Signal Processing
- **FPGA design internships/MEng project at pureLiFi**
- **Embedded SW Engineer at Monitor Audio for a year**
- **Joined Cirrus Logic as Verification Engineer in 2020**

Work Culture

Cirrus Logic is proud to be recognized
globally as a top workplace for our corporate culture
and our environmental commitment .

CIRRUS LOGIC®

TOP WORK PLACES 2010
TOP WORK PLACES 2011
TOP WORK PLACES 2012
TOP WORK PLACES 2013
TOP WORK PLACES 2014
TOP WORK PLACES 2015
TOP WORK PLACES 2016
TOP WORK PLACES 2017
TOP WORK PLACES 2018
TOP WORK PLACES 2019
TOP WORK PLACES 2020
Austin American-Statesman statesman.com

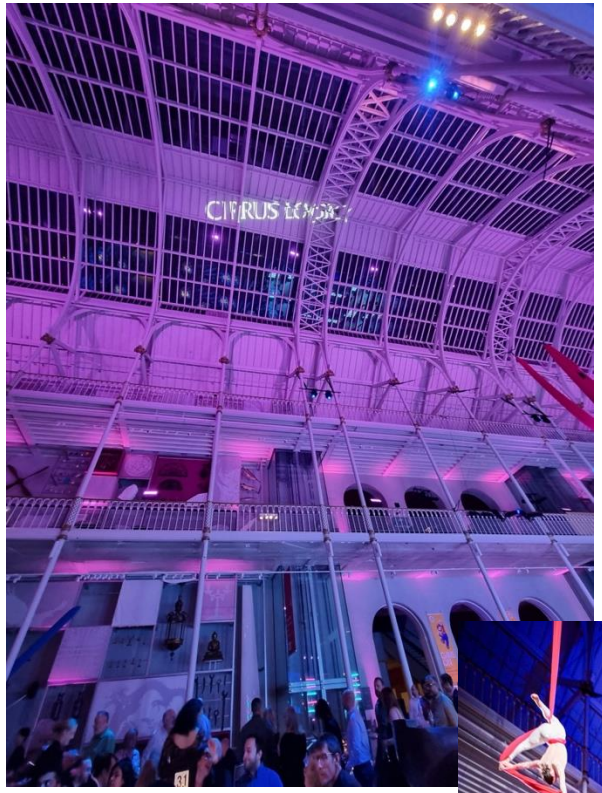
Best Workplaces™ Large Organisations
Great Place To Work. UK 2020

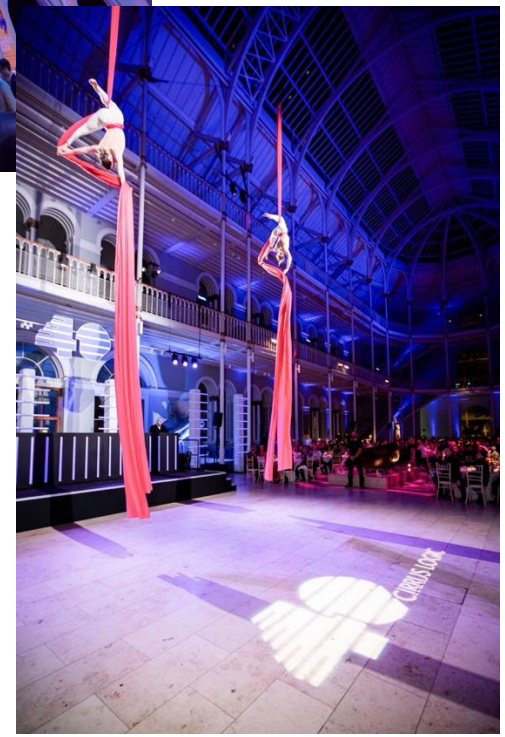
Best Workplaces™ in Texas
Great Place To Work. USA 2020

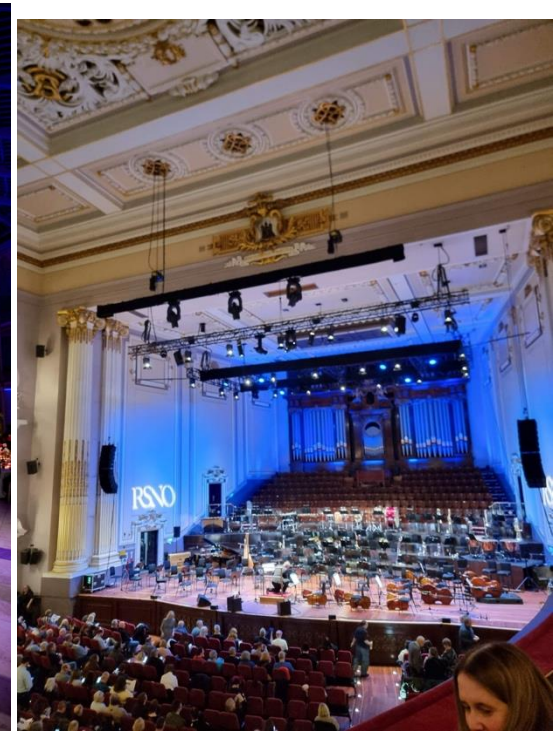
SONY GREEN PARTNER

SUSTAINABLE DEVELOPMENT GOALS

Cirrus







- Xmas party
- Office gym & practice room
- Sponsors Edi Science Festival
- Sponsors Edi Usher hall
- Monthly happy hour
- Monthly birthday cake
- Breakfast and lunch
- Prize draws

CIRRUS LOGIC



Marshall





TRAKTOR AUDIO 6
TRAKTOR

AMP
EQ
EFFECTS
MODIFY
Fender
MUSTANG MICRO

Astell&Kern



08:08


Cambridge Audio
DacMagic 100
Digital to Analogue Converter

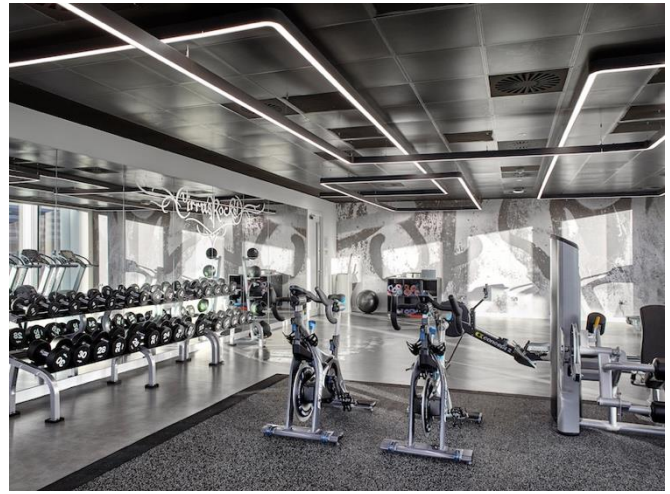
BOSE

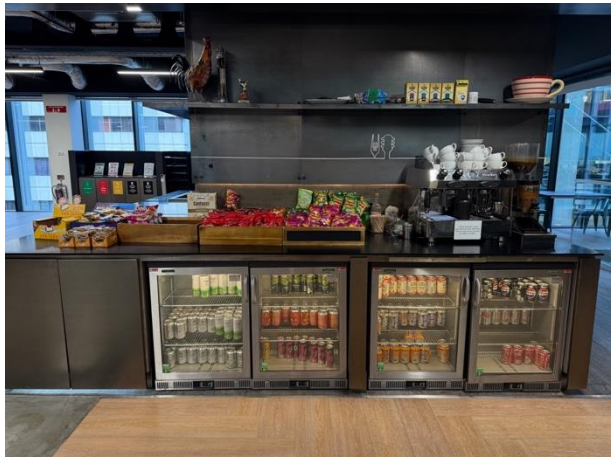
12:25
SAMSUNG

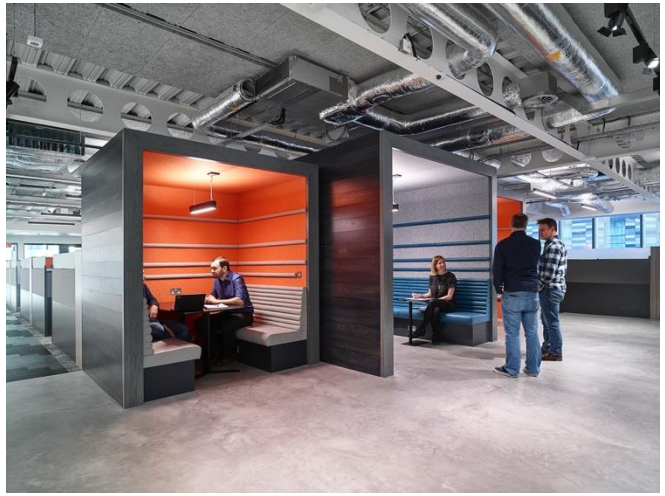
Nikon
D3500

Solar Intensity
Last 6 Hours


Edinburgh Office







CIRRUS LOGIC

Benefits of the industry

- Good pay from the get-go
- Bonus

Experience	Graduate MSc	Graduate PhD	Mid-level 2-5yrs	Senior 6-10yrs	Principal 11-15yrs	Senior Principal 12-20yrs	Technical Team Lead 15+yrs	Technical Manager (team of 5+ engs)	Eng. Director/ Design Centre Manager/ VP Eng
Digital IC Design	£38-45,000	£45-50,000	£50-55,000	£55-70,000	£70-80,000	£80-90,000	£85-95,000	£95-130,000	£130,000+
Digital IC Verification	£38-45,000	£45-50,000	£50-55,000	£60-75,000	£75-85,000	£85-95,000	£95,000+	£95-130,000	£130,000+
Physical Design	£38-45,000	£45-50,000	£50-55,000	£55-70,000	£70-80,000	£80-90,000	£85-95,000	£95-130,000	N/A
FPGA Design	£38-45,000	£45-50,000	£50-55,000	£55-70,000	£70-80,000	£80-90,000	£85-95,000	£95-130,000	N/A
Analog/Mixed Signal IC Design	£38-45,000	£45-50,000	£50-55,000	£55-70,000	£70-80,000	£80-90,000	£85-95,000	£95-130,000	£130,000+
RF IC Design	£38-45,000	£45-50,000	£50-58,000	£58-75,000	£75-85,000	£85-95,000	£85-100,000	£100-130,000	£130,000+
Analog / RF Layout	£35,000	£35-38,000	£38-50,000	£50-65,000	£65-70,000	£70,000+	£70,000+	£85-95,000	N/A
IC Test	£30-35,000	£30-37,000	£37-45,000	£45-55,000	£55-70,000	£70-80,000	£80-90,000	£90-100,000	£100,000+
IC Process	£28-33,000	£28-35,000	£35-42,000	£42-50,000	£50-60,000	£60-65,000	£65-70,000	£70-80,000	£80,000+

Salary Ranges in the Semiconductor Industry in the UK, 2022

https://ic-resources.com/en/upload/salary-guides-34-pdf-salary-20review-202022-20q3-20q4-pdf-utm-source-paiger-amp-utm-medium-referral

Graduate life in Cirrus – Ben

- STMicroelectronics industrial placement
- FPGA in the loop
- MATLAB HDL ML synthesis and deployment
- Focused on deep learning at HWU
- New to verification

cadence

O'REILLY

coursera

TechNES

DOULOS

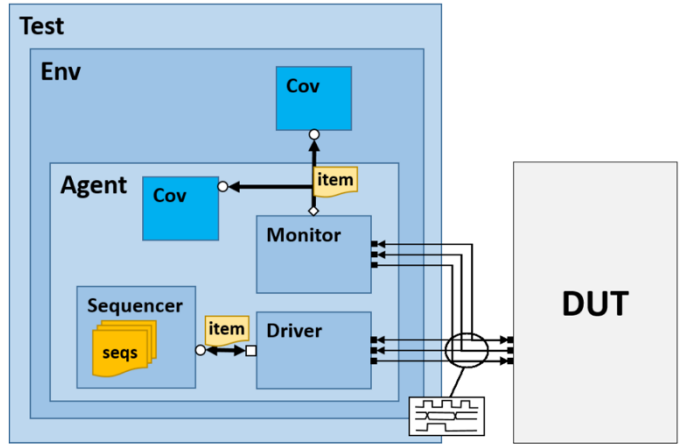
SIEMENS Verification Academy

Confluence

Jira

Jenkins

RMS Project



UVM

Graduate life in Cirrus – Ben

---------- Year 1 ----------

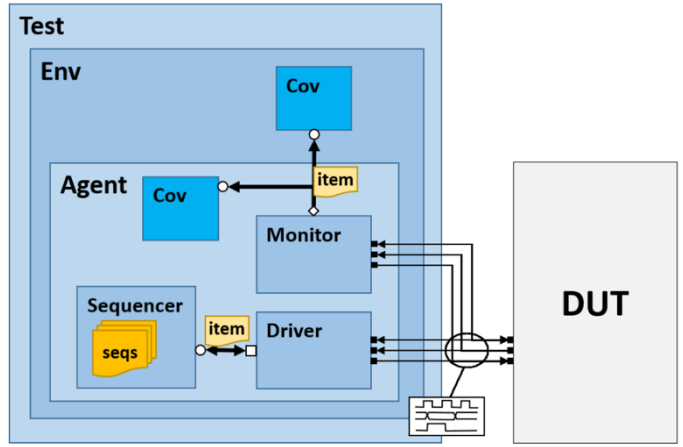
- New to SystemVerilog and verification
- First 3 months tutorials on UVM & SystemVerilog
- Handheld through initial tasks in UVM
- IP development - 3 months of SystemVerilog, UVM, SVA implementation
- Start on a project from the ground-up – 11 months

Confluence

Jira

Jenkins

RMS Project



UVM

CIRRUS LOGIC

Graduate life in Cirrus – Ben

- ---------- Year 2 ----------
- Worked more independently,
- creating a VIP for from the ground-up
- Updating of legacy testbench

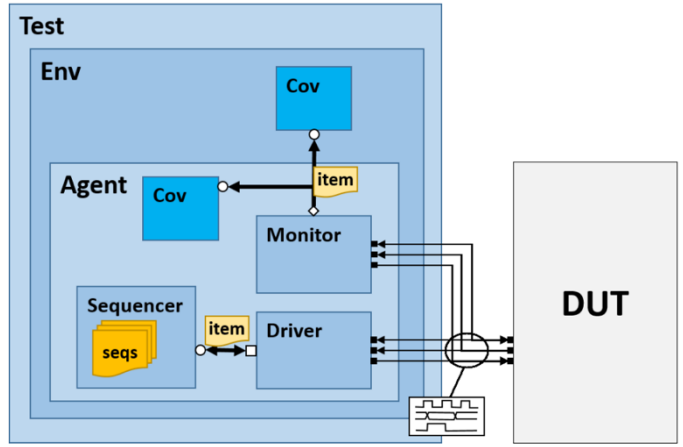
- Goal setting and supported in self development

Confluence

Jira

Jenkins

RMS Project



UVM

Graduate Life In Cirrus – Vlad

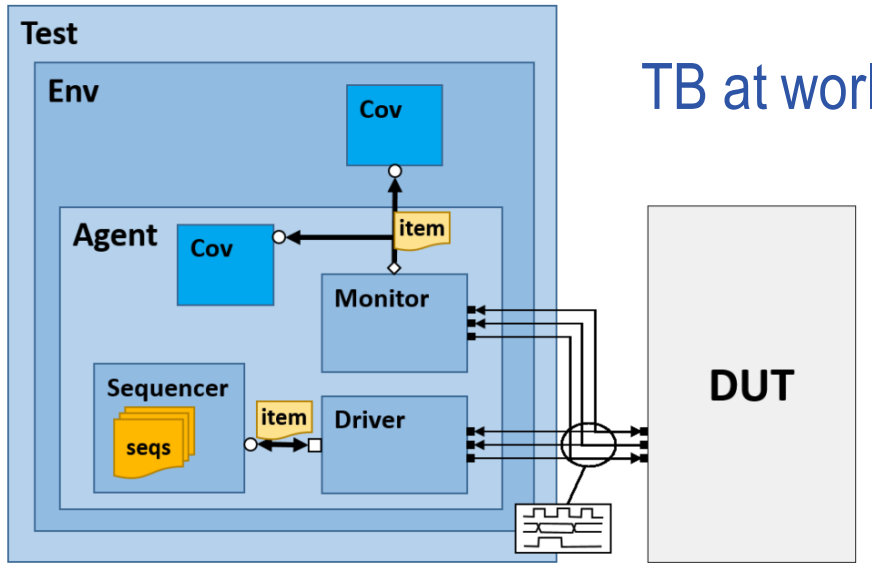
- **Part 1 – Training** (~6 months)
- Completely new to Digital Verification
  1. UVM (Universal Verification Methodology) and SystemVerilog training
  2. Picking up small tasks on projects
  3. Understanding Cirrus internal tools
  4. Learning how to debug Digital and Mixed Signal Designs
- **Key Takeaways:**
  - Verification is like Software Engineering but using an HDL
  - More coding than Digital designers
  - Possibilities for learning are vast

```
initial begin
  d <= 0;
  en <= 0;
  rstn <= 0;
  // 2. Release reset
  #10 rstn <= 1;
  // 3. Randomly change d and enable
  for (i = 0; i < 5; i=i+1) begin
    delay = $random;
    delay2 = $random;
    #(delay2) en <= ~en;
    #(delay) d <= i;
  end
end
```

TB at Uni

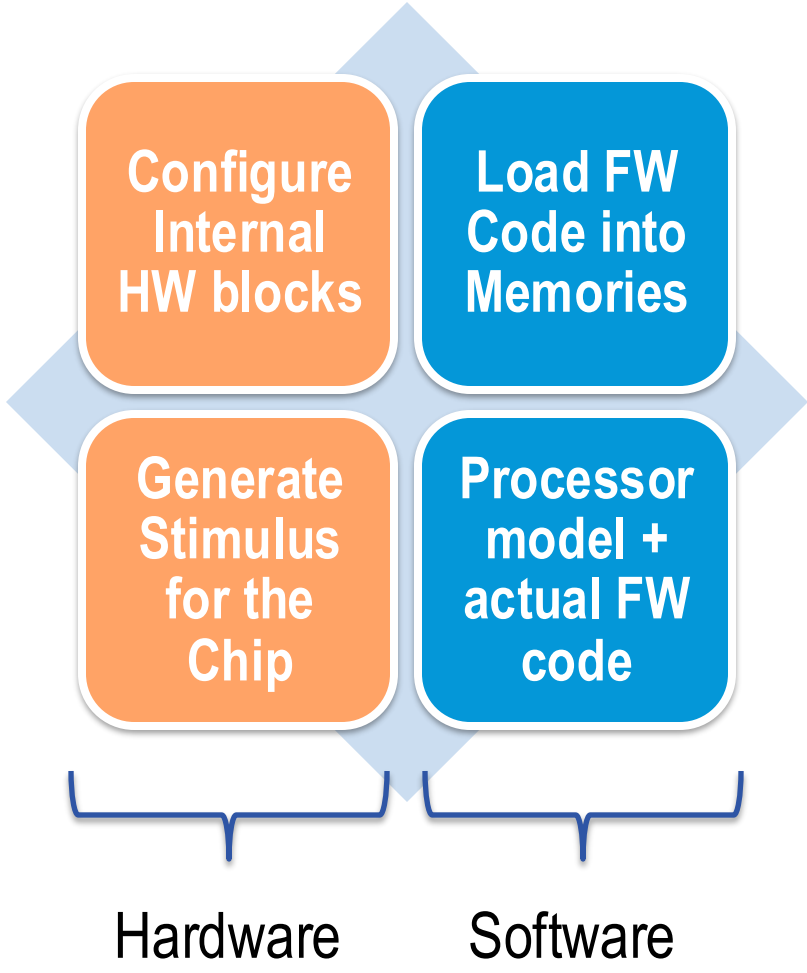
Training

TB at work



Graduate Life In Cirrus – Vlad

- **Part 2 – First Projects**
  - HW/SW Co-Verification – writing stimulus for Cirrus DSP
    - SystemVerilog, C, Matlab
  - Digital Verification
    - Bus protocols, Clock generation, FIFOs, etc.
  - Mixed Signal verification
    - Hybrid PLLs, DLLs, DACs



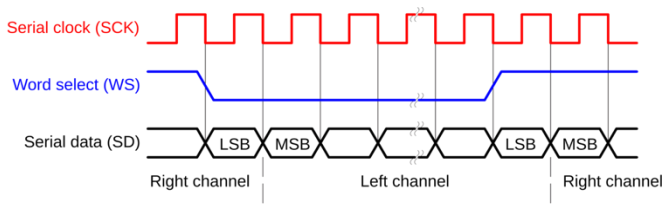
Graduate Life In Cirrus – Vlad

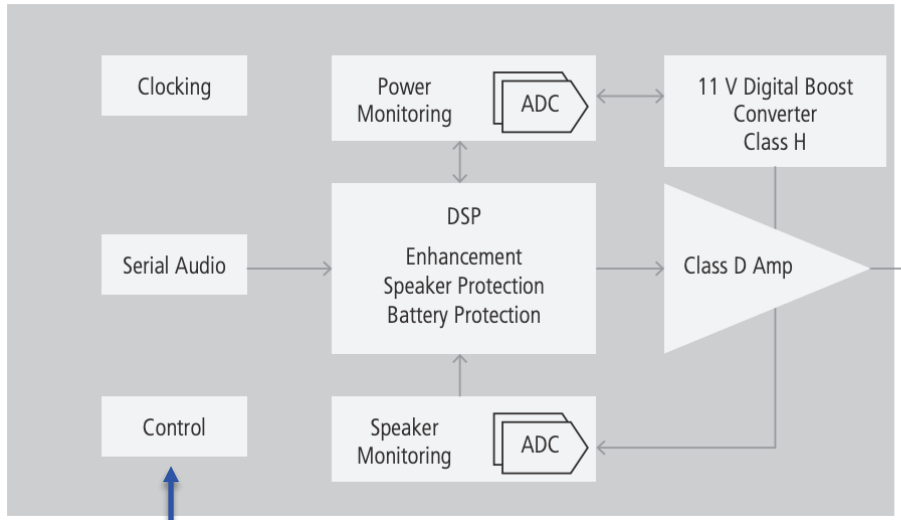
- **Part 3 – Where I am Now**
  - Chip verification lead
    - Working with designers, systems architect and other teams to define verification strategy
    - Overseeing work of 5 verification engineers
    - Taped out recently and shipping to customers☺
  - Testbench Lead
    - Coming up with Testbench architecture for a chip
    - Outlining required test environment components

Graduate Life In Cirrus – Vlad

- Verification is not just about writing tests!
- You define the environment around the chip:

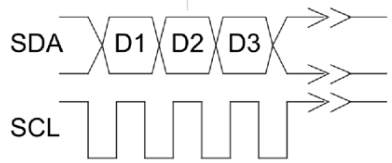
I2S VIP





Matlab Checks, Eg. FFT

I2C/SPI Control Interface VIP



Questions

Past projects | Interviews

Important Dates

Contact

Vlad

www.linkedin.com/in/vladislav-rumiantsev

Vladislav.Rumiantsev@cirrus.com

Ben

https://uk.linkedin.com/in/ben-harper-5a229016

Ben.Harper@cirrus.com

Online

http://www.cirrus.com/careers/students

References

- https://www.analog.com/en/resources/technical-articles/i2c-primer-what-is-i2c-part-1.html
- https://en.wikipedia.org/wiki/I%C2%B2S
- https://www.tessolve.com/verification-futures/vf2022/hardware-software-co-verification-101/
- https://verificationacademy.com/cookbook/uvm-universal-verification-methodology/