Mixed Signal Soc Verification

DVClub Edinburgh

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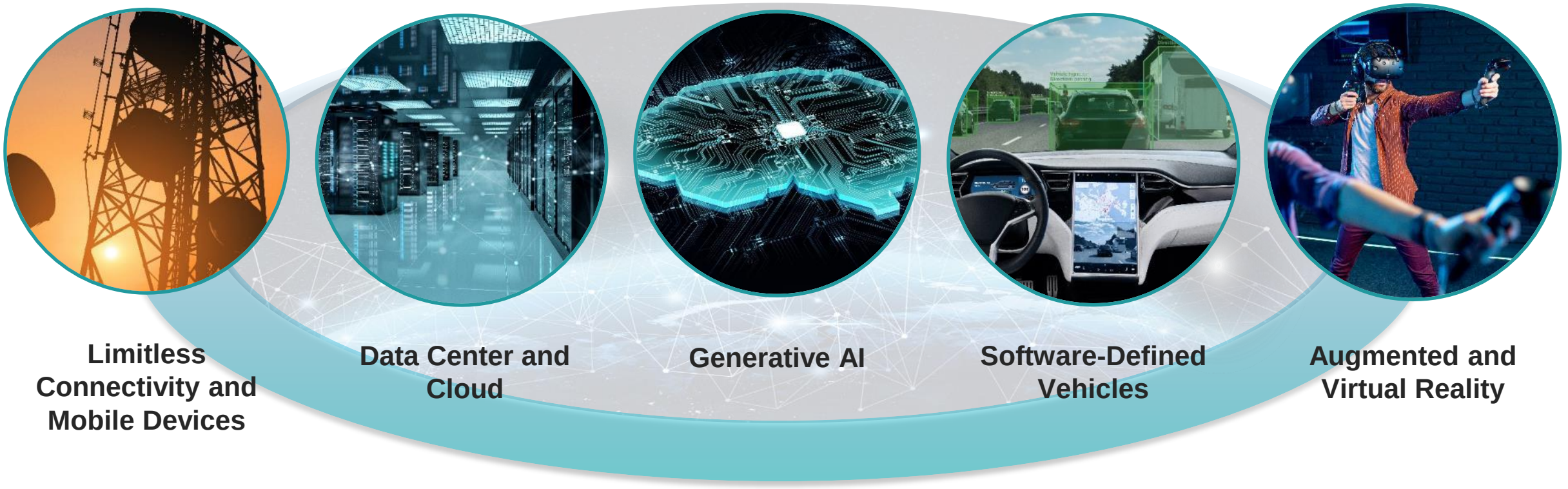
cadence®

Presentation Outline

- Introduction
- Mixed Signal Verification
- Cadence Tool Suite for Mixed Signal Verification
- Mixed Signal Verification Debugging
- Cadence Mixed Signal Verification Innovations
  - Palladium and RNM
  - Jasper
- Customer Success Stories
- 2025 Cadence Mixed Signal Verification Vision
- Summary

Computer Chips Are Powering Everything



Limitless Connectivity and Mobile Devices

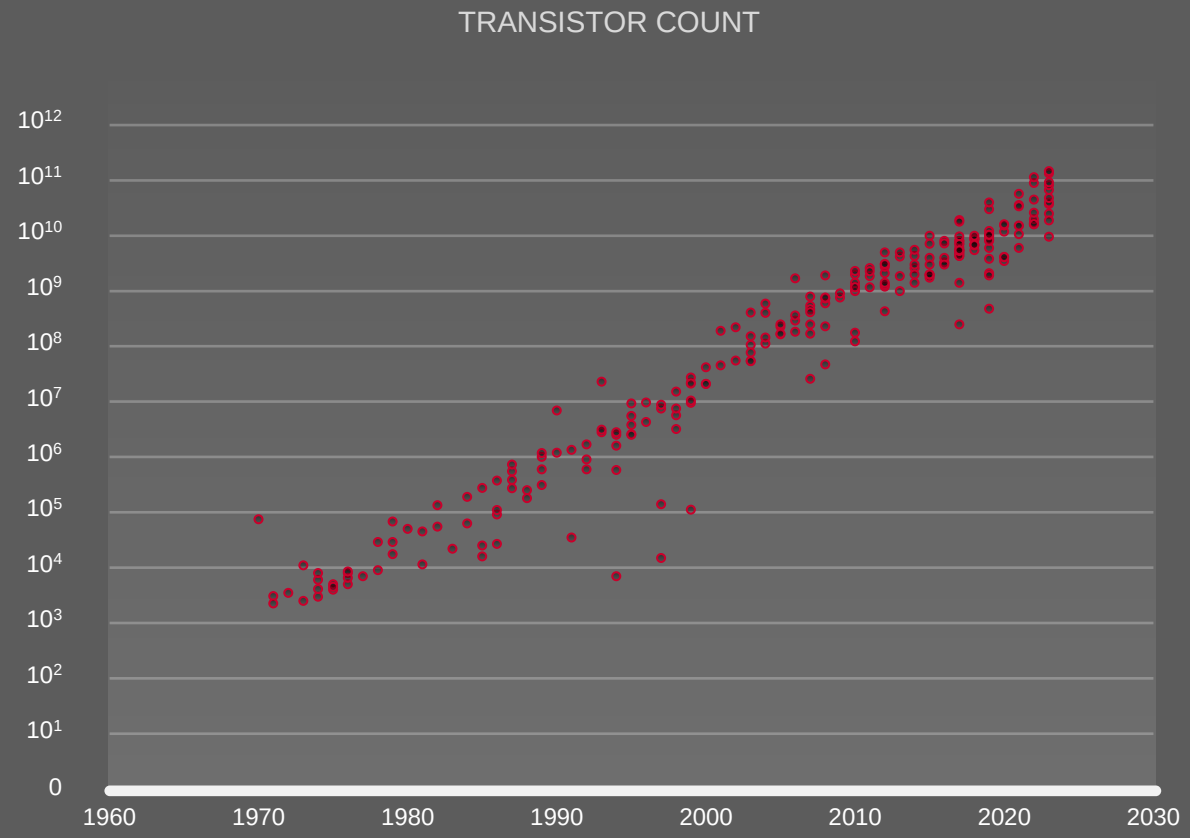
Data Center and Cloud

Generative AI

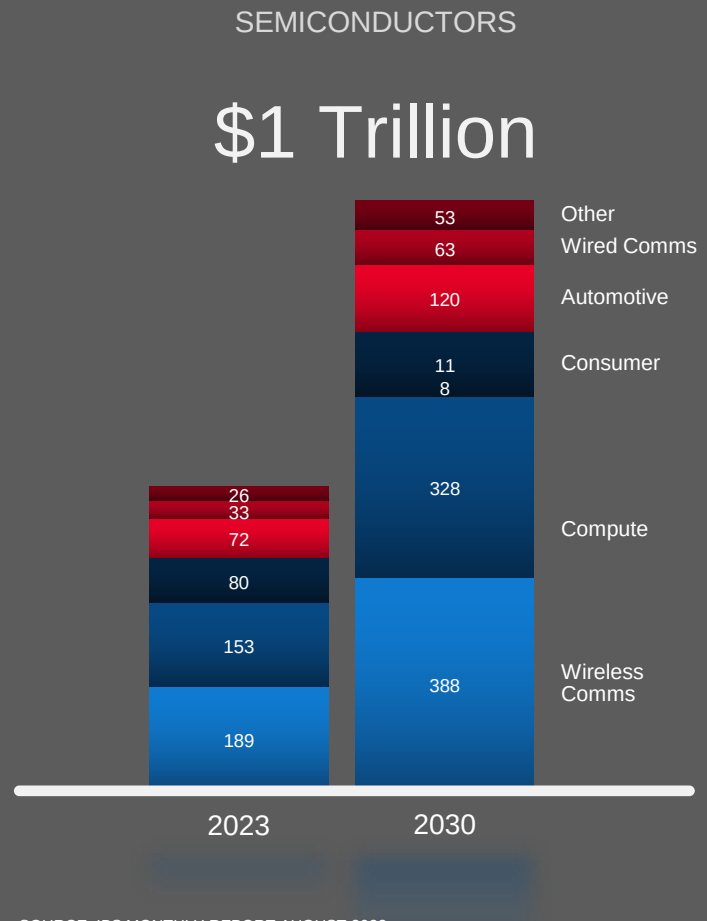
Software-Defined Vehicles

Augmented and Virtual Reality

The Future Is Bright for Semiconductors

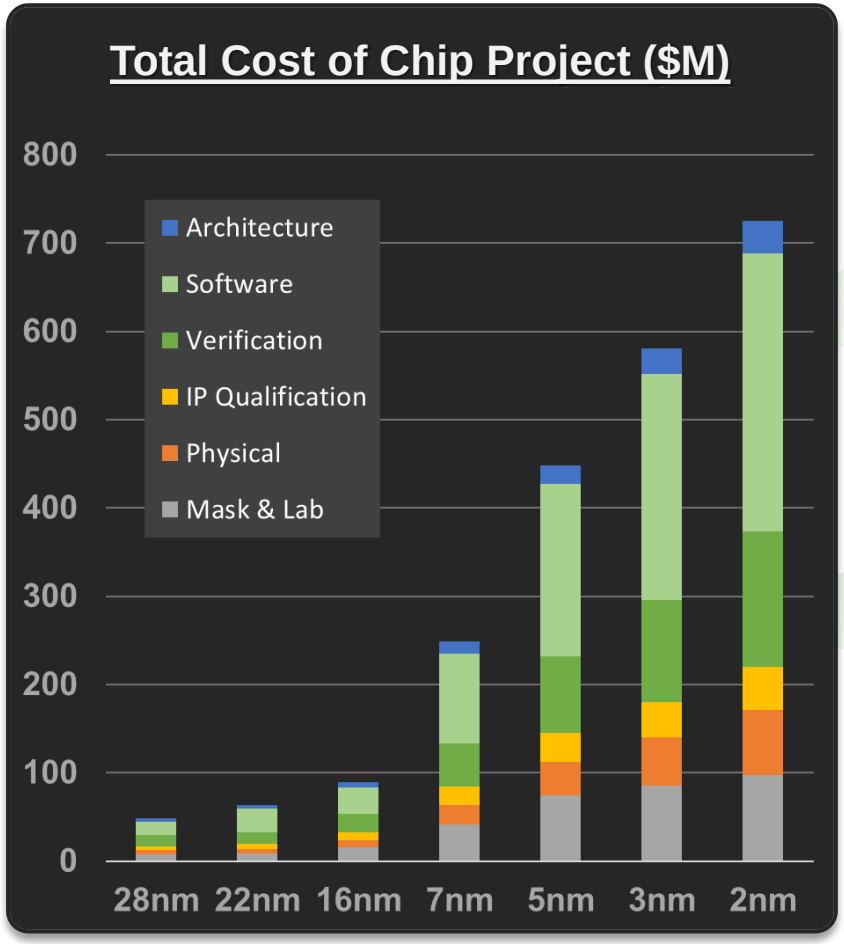


SOURCE: WIKIPEDIA "TRANSISTOR COUNT"



SOURCE: IBS MONTHLY REPORT AUGUST 2023

Verification Strategy



IBS, Global Semiconductor Industry Service Report, July 2022

Pre-Silicon Software Validation

Dynamic Duo of Cadence Silicon and FPGA-based hardware acceleration

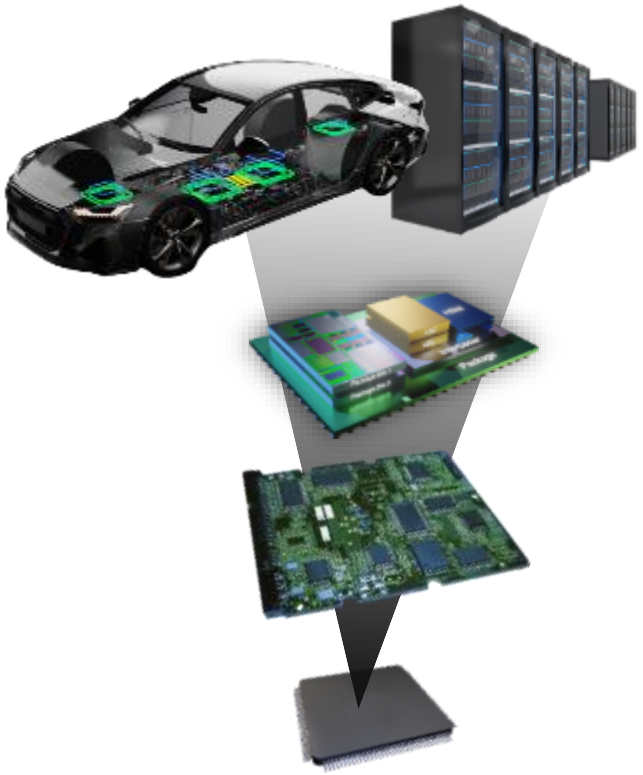
Chip Verification

Lead in verification performance with the fastest engines and an AI-driven full flow

ROI Mindset
bugs found per $ per day

Cadence Overview

Leading provider of **Intelligent System Design**™ solutions software, hardware, and IP that turn design concepts into reality



Computational software
for designing today's electronic systems

$1.215B
Q3 2024 revenue

>12,000
employees worldwide

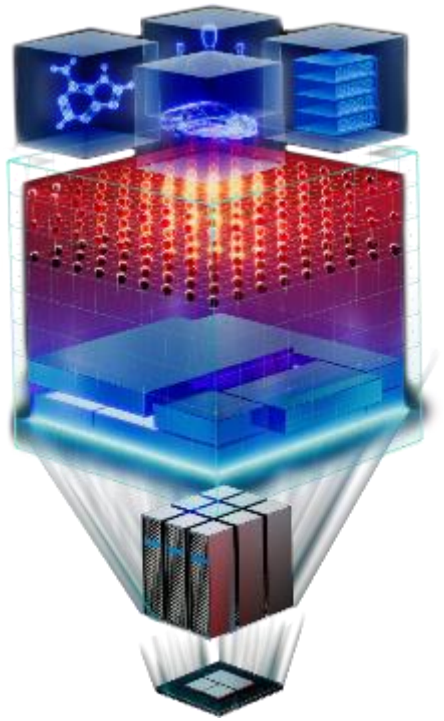
Culture of innovation
more than 20 significant new products in last 3 years

26
global development centers

Nasdaq: CDNS; S&P 500 and Nasdaq 100 indexes

Source: Cadence Earnings Press Release, October 28, 2024
https://www.cadence.com/en_US/home/company/newsroom/press-releases/pr-ir/2024/cadence-reports-third-quarter-2024-financial-results.html

Cadence Accelerated Design Solution



cadence.ai

Cadence® Cerebrus™ | Virtuoso® Studio | Verisium™ | Optimality™ | Allegro® X AI | •••

AI

EDA: Digital | Custom | Verification

SDA: 3D-IC | PCB | Multiphysics

Environmental: Data Center Digital Twin

BIO: Molecular Science

•••

Principled Simulation + Optimization

Cadence Palladium® | Cadence Protium™ | Cadence Millennium™

X86 CPU | Arm® CPU | FPGA

GPU | NPU | Cadence IP

•••

Accelerated Compute

Mixed-Signal Verification

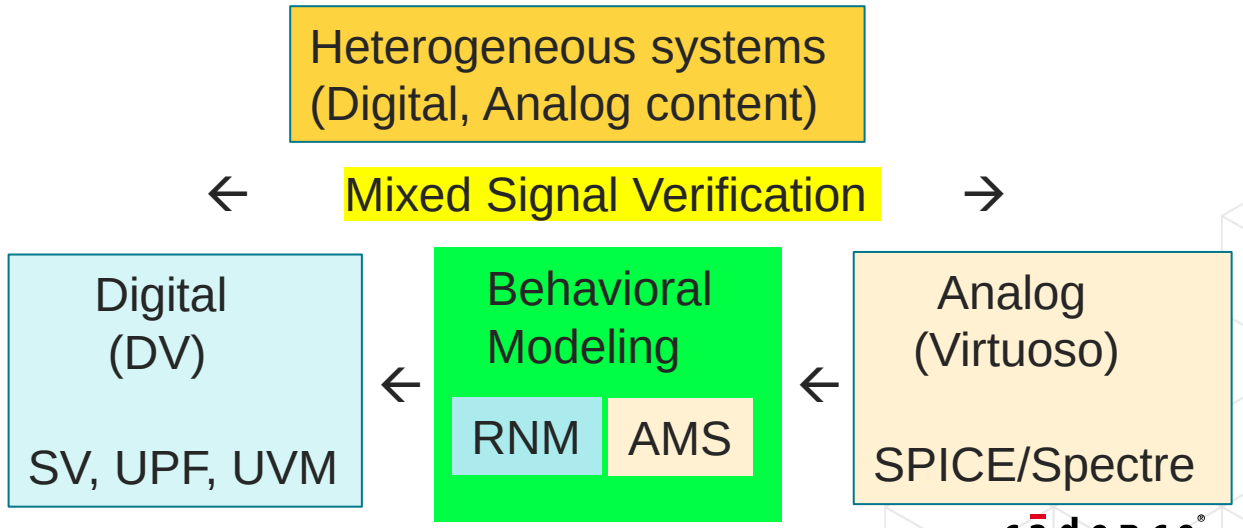
Mixed-Signal Simulation Essential to Today's SoCs

- SoCs increase in analog blocks
  - 5G LTE, AI/ML, IoT, Haptics
- Analog/Digital interaction needs to be verified
  - Not testing interaction leads to failures
  - Mixed-Signal bug finding accelerated by regressions
- SoC / SPICE co-sim doesn't scale
  - SPICE fidelity / performance trade-off prevents needed verification
  - SV Real Number Modeling approaches accuracy at digital simulation speeds
    - Runtime improvement of 100x-1000x

- More "connected" -> WiFi / Bluetooth / RF
- Everything "smarter" / Intelligent -> Sensors
- Need all day / Power management -> PMICs

New Design Concepts to Reality!

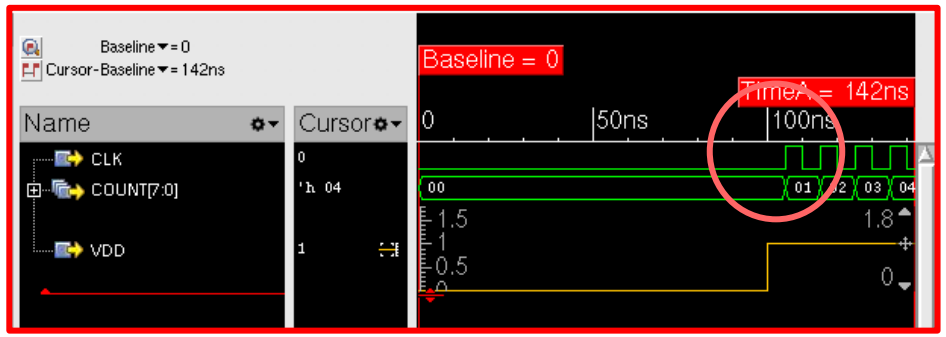
IP (Blocks) <-> Chips (SoCs) <-> Systems



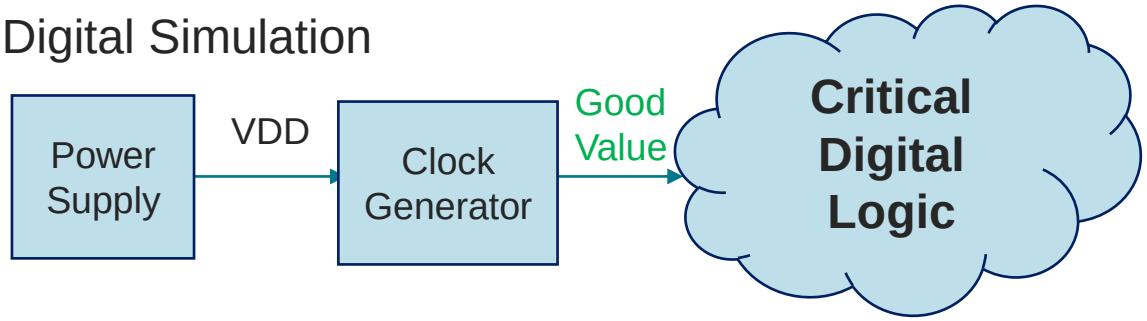
Applications of Mixed-Signal Verification

- Complex analog control with high-speed clocks
  - From Analog to Digital or Digital to Analog interaction
    - Large number of states required in digital for analog conversion
  - Non linearities in A to D conversion, over voltage, over current detection, PLL clock drifts, over temperature conditions, …
- Power supply sequencing
  - Verifying transition of Power States
  - Is PLL lock tracked properly
- Low power modes
  - Power supply loading, brown out when sequencing is incorrect, ...

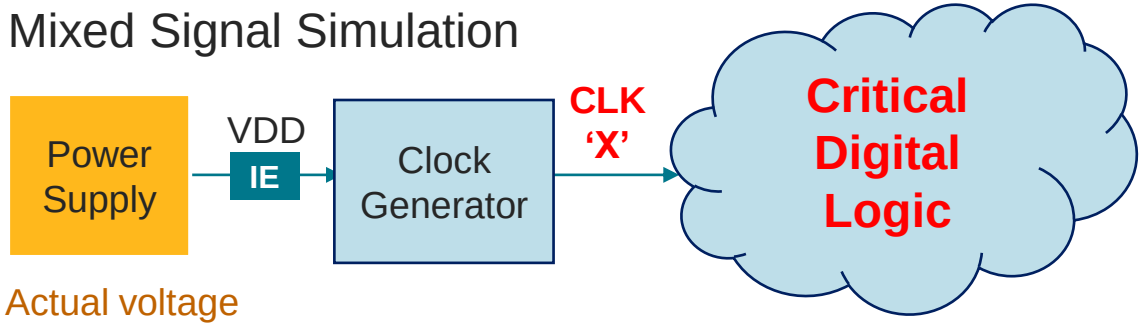
Find Bugs Earlier in Verification



Digital Simulation



Mixed Signal Simulation



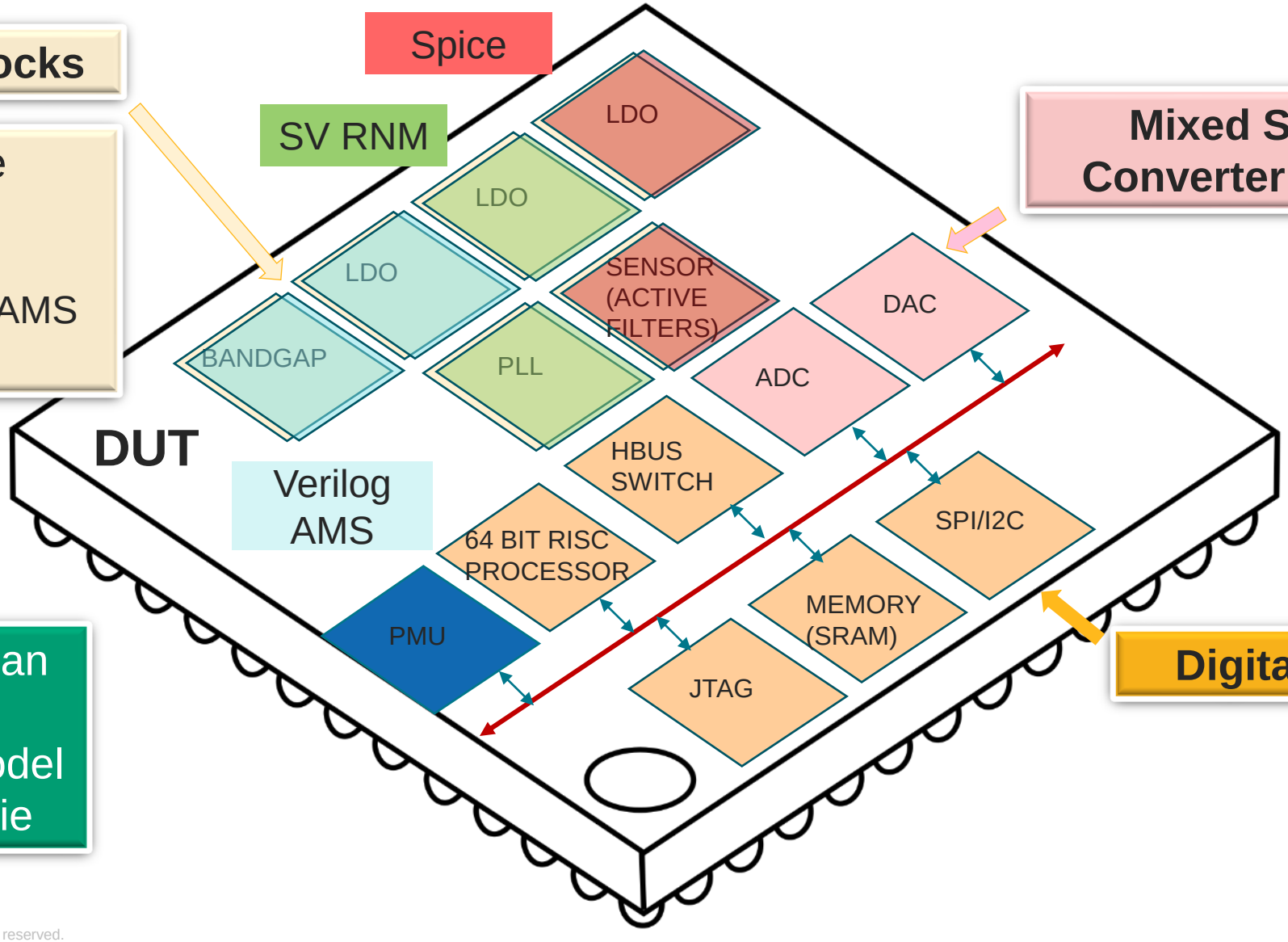
Actual voltage
RNM domain

The issue was found due to ramp-up of VDD Voltage in MS which Digital Simulations missed

Mixed Signal Soc

Analog Blocks

Analog Blocks can be
- Spice (Co-sim)
- SVRNM, VHDLRNM
- Verilog-AMS, VHDL-AMS
- C, SystemC



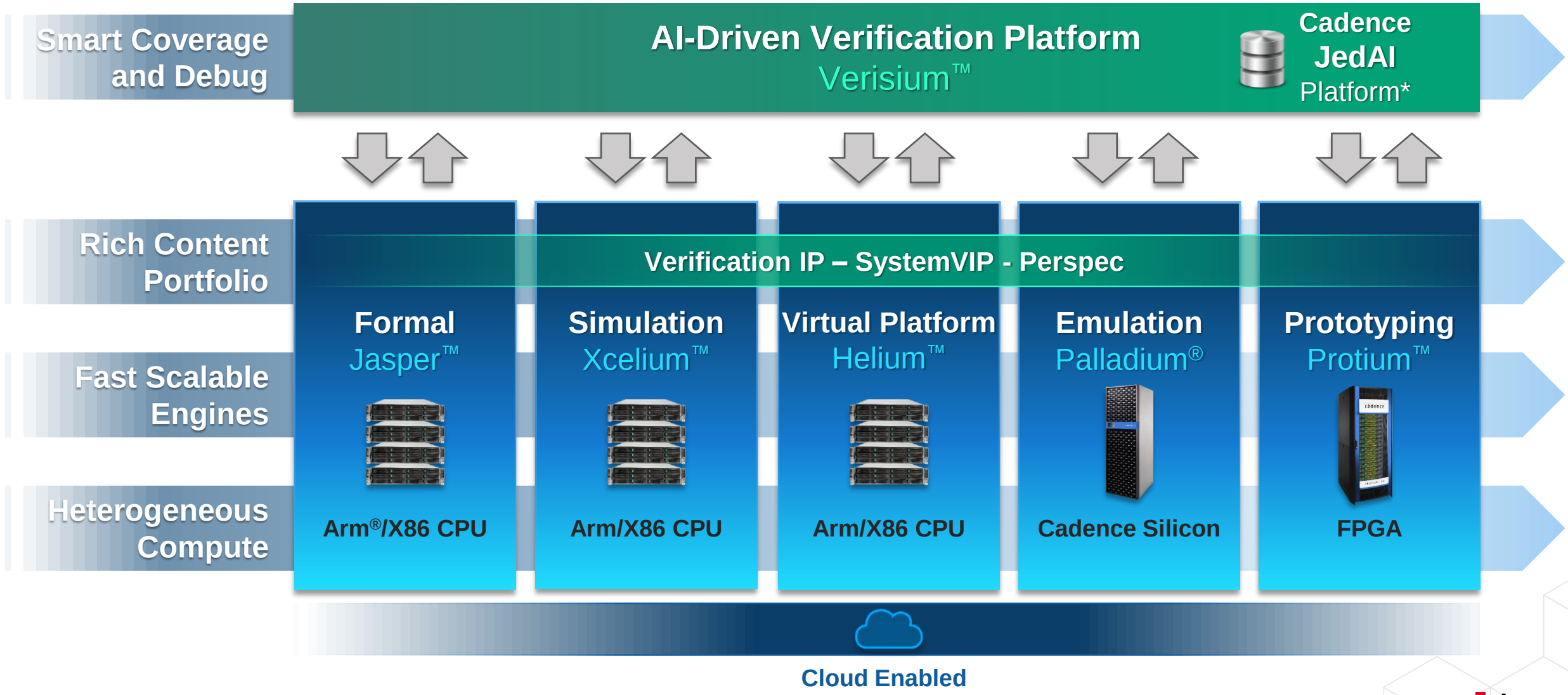
Mixed Signal Converter Blocks

Digital Blocks

Seamlessly user can mix and match different Analog model abstractions (Spcie

Cadence Tool Suite for Mixed Signal Verification

Optimizing Throughput Across The Full Verification Flow

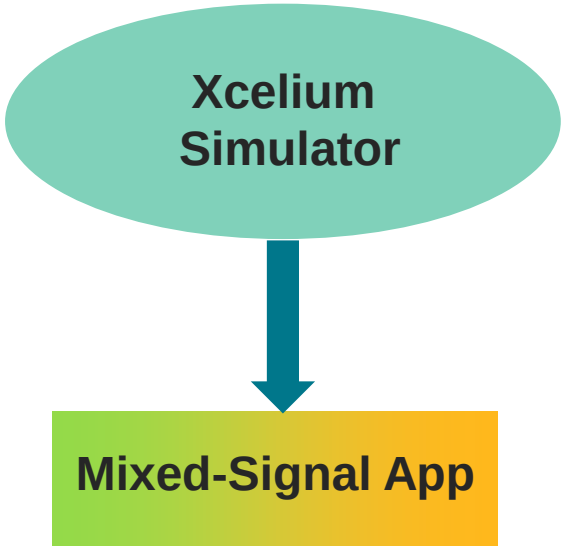


* Cadence® Joint Enterprise Data and AI (JedAI) Platform

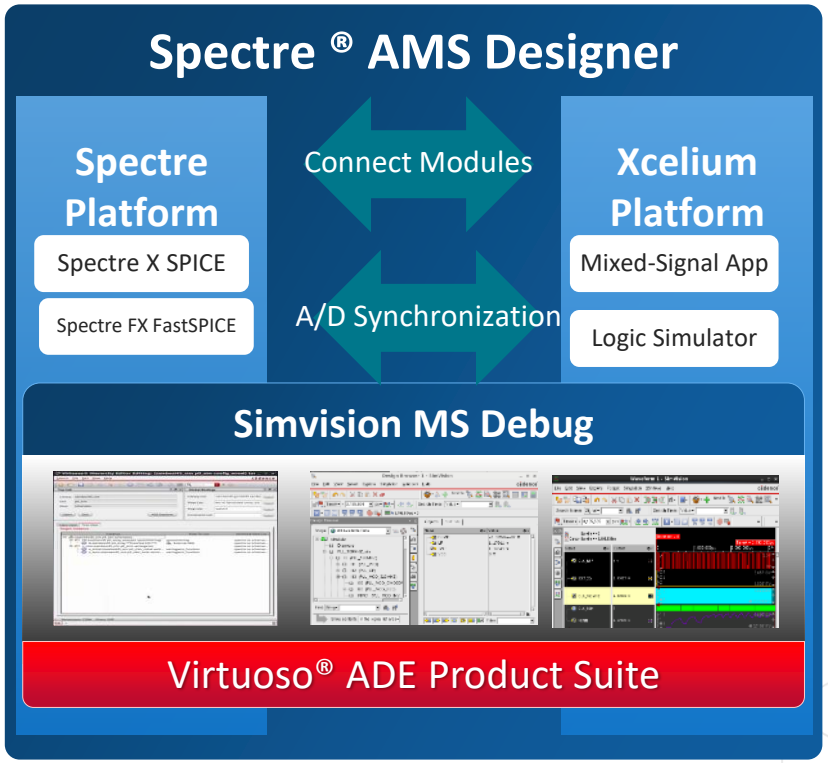
Xcelium Mixed-Signal App

- The **Xcelium™ Mixed-Signal App** enables mixed-signal simulations for:
  - DV Applications: Enables event based digital mixed-signal simulation with RNM
  - AMS Applications: Integrated with Spectre™ AMS Designer to enable mixed signal simulation for co-simulation or AMS Applications

RNM / DV Applications

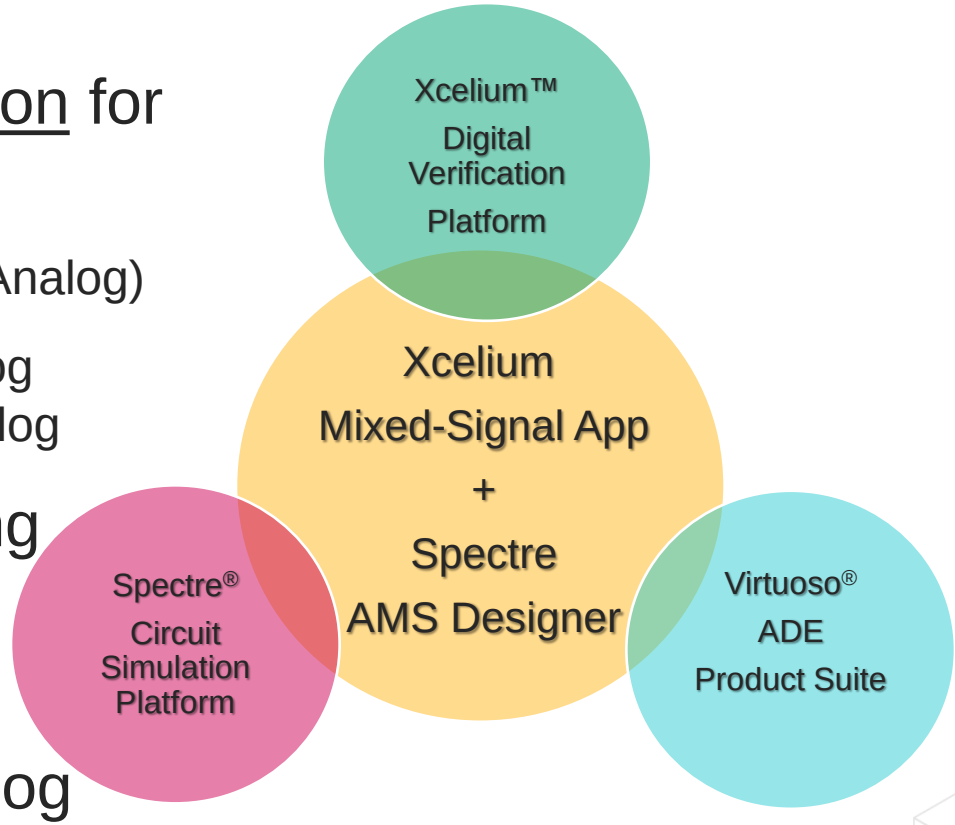


Co-sim / AMS Applications



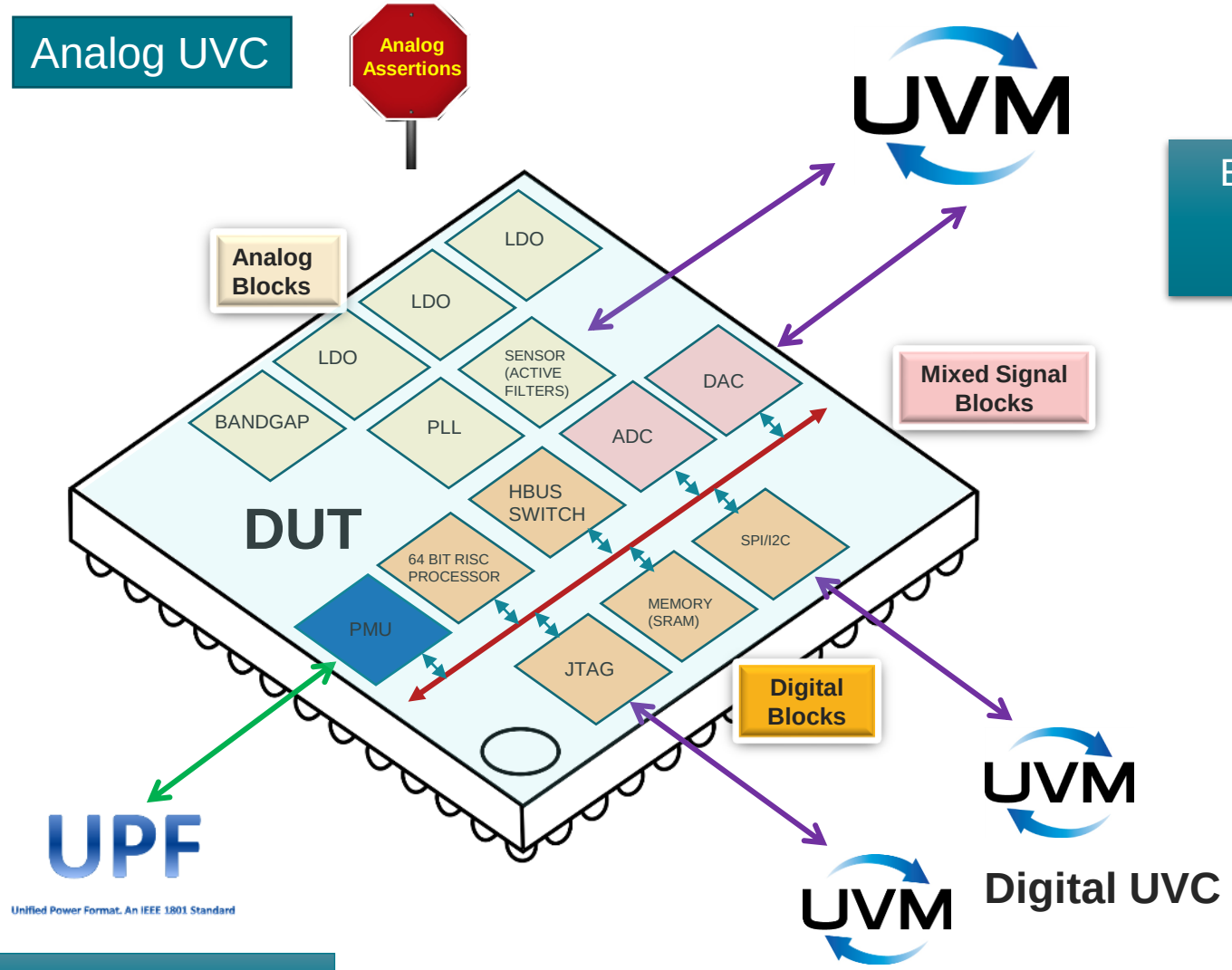
For High Performance, Seamless Mixed-Signal Verification

- Single mixed-signal elaboration and simulation solution for complex SoCs and multi-chip designs
  - Common MS simulator within *domain-specific* environments (DV, Analog)
  - Seamless use model in both command-line/DV and Virtuoso/Analog environments for highly productivity hand-off between DV and Analog
- Simulation planning, regression, and traceability using Verisium Manager™ Metric-Driven Signoff Platform
- Use with Virtuoso ADE Assembler and Verifier for simulation management and distribution with an analog point of view



Full Flow Verification with Xcelium Mixed-Signal App

Analog UVC



Enable Metric Driven Verification (MDV), Verisium Manager

Use Verification Capabilities in MS

- Connect UVM objects to analog components
- Advanced MDV concepts with MS designs (features also works with Spice)
- Use System Verilog efficiencies to create replicated instances with analog blocks

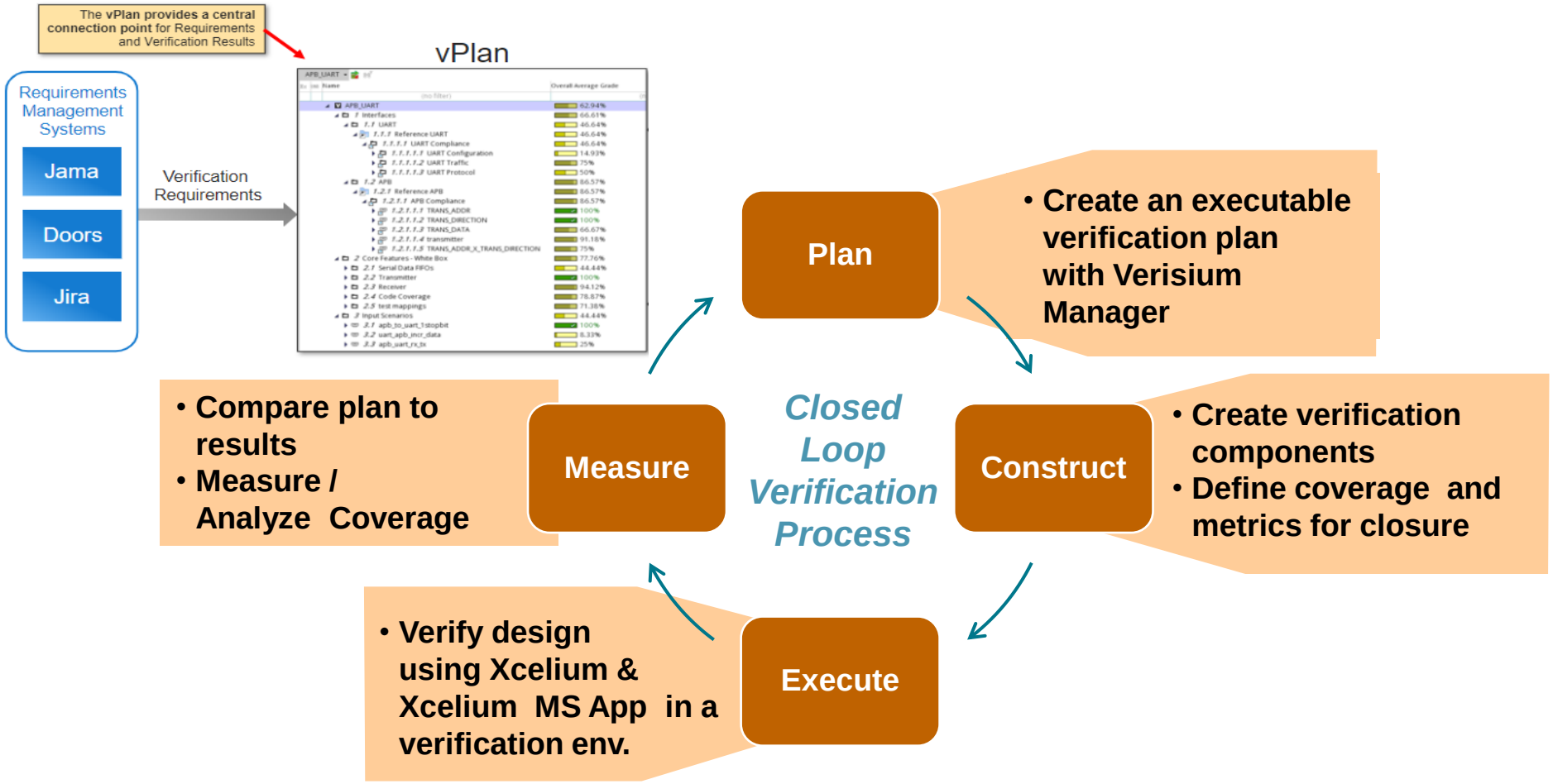
Digital UVC

Apply Low Power

Use existing UVM test benches

Advanced MS SoC Verification Methodology

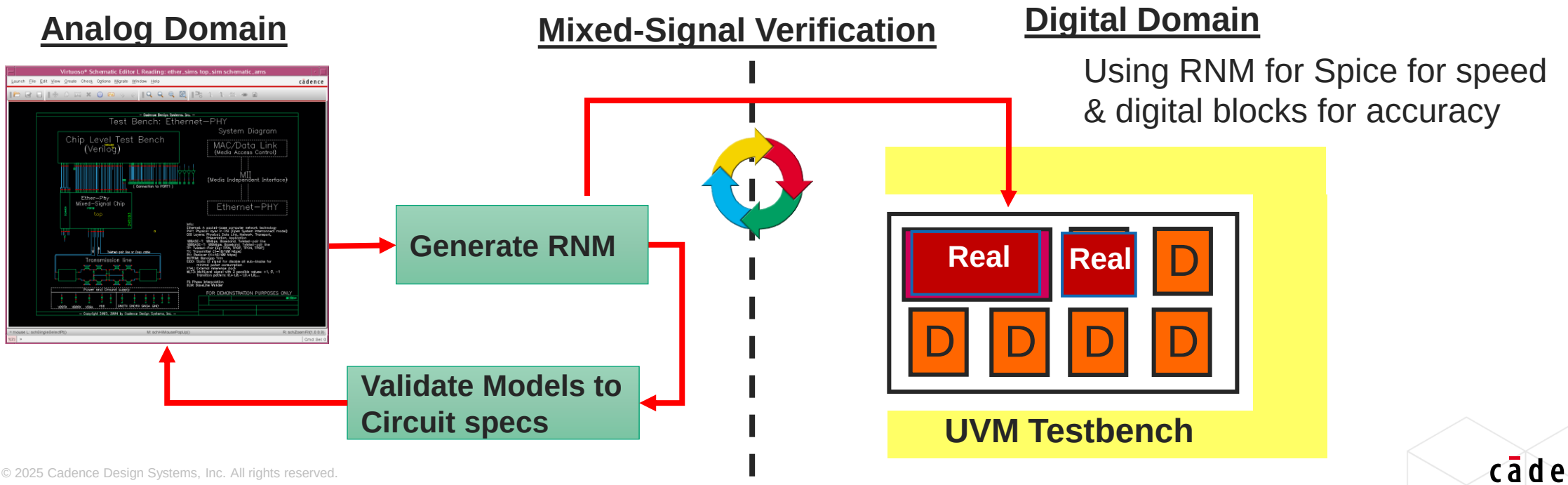
Metric Driven Verification (MDV) Flow



The MDV solution allows users to proactively manage verification metrics, enabling users to close the verification loop faster

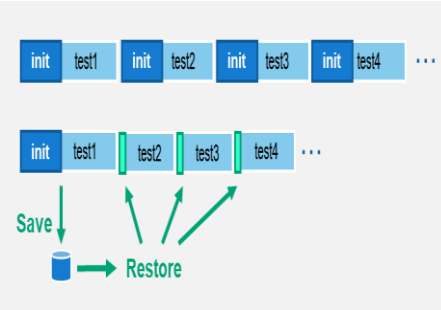
Real Number Modeling, (RNM) for Mixed-Signal Simulation

- The designs have greatly increased in size and cannot be simulated in pure SPICE simulation
  - Traditionally analog designer using a SPICE simulator to verify their design
- SV RNM executes analog 100x to 1000x faster in Xcelium running system-level tests
- SV RNM also enable simulation with high accuracy
- Models are easily ported between Virtuoso® and Xcelium environments



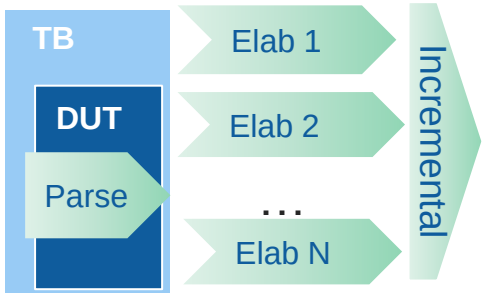
Xcelium: Leadership digital mixed-signal Performance

Save & Restore



Init once across multiple tests

Incremental Build

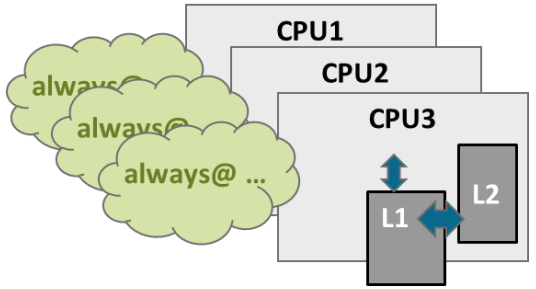


Rapid iteration using MSIE

SimAI

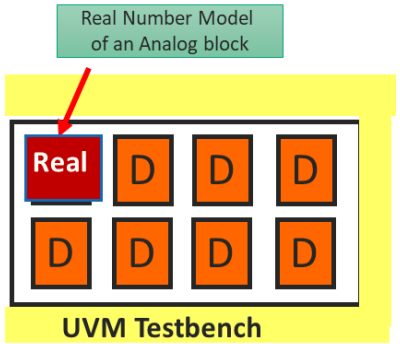
3-5X on randomized testsuites

Multi-core Technology



3-5X on gate-level DFT sims

Real Number Modeling

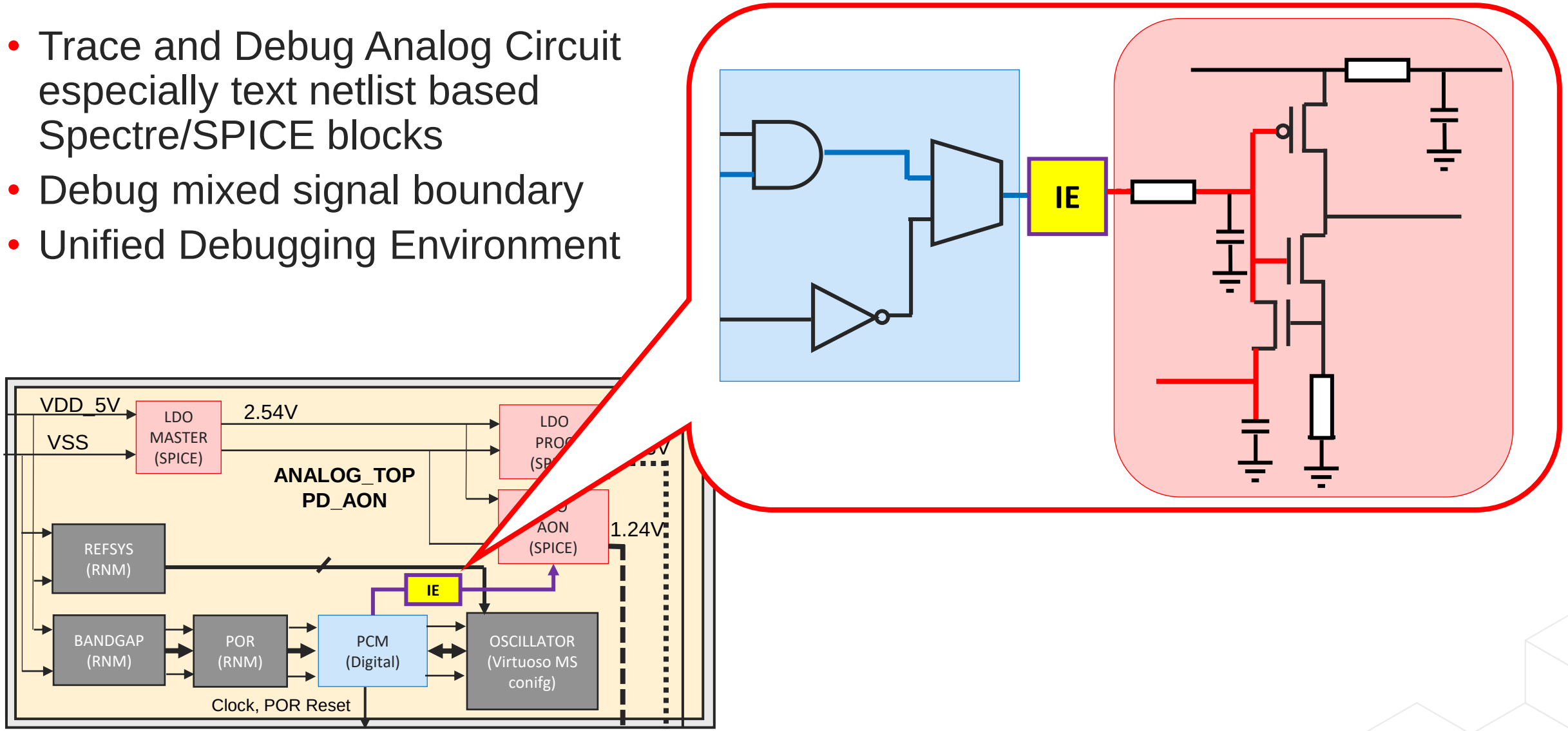


Leading performance / EEnet Library

Mixed Signal Verification Debugging.

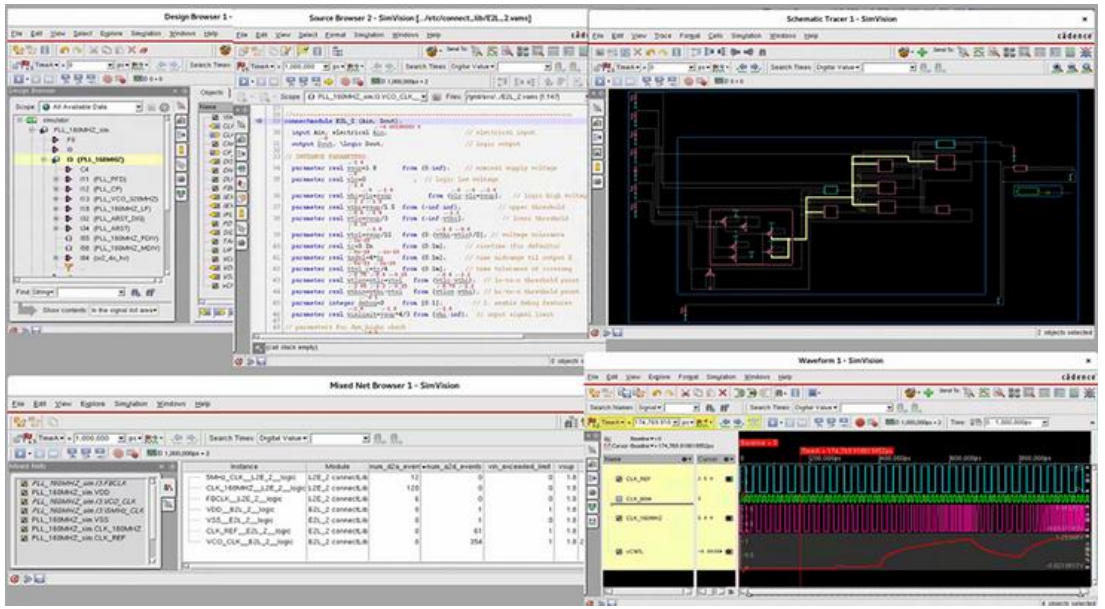
Analog and Mixed Signal Debugging Challenge

- Trace and Debug Analog Circuit especially text netlist based Spectre/SPICE blocks
- Debug mixed signal boundary
- Unified Debugging Environment

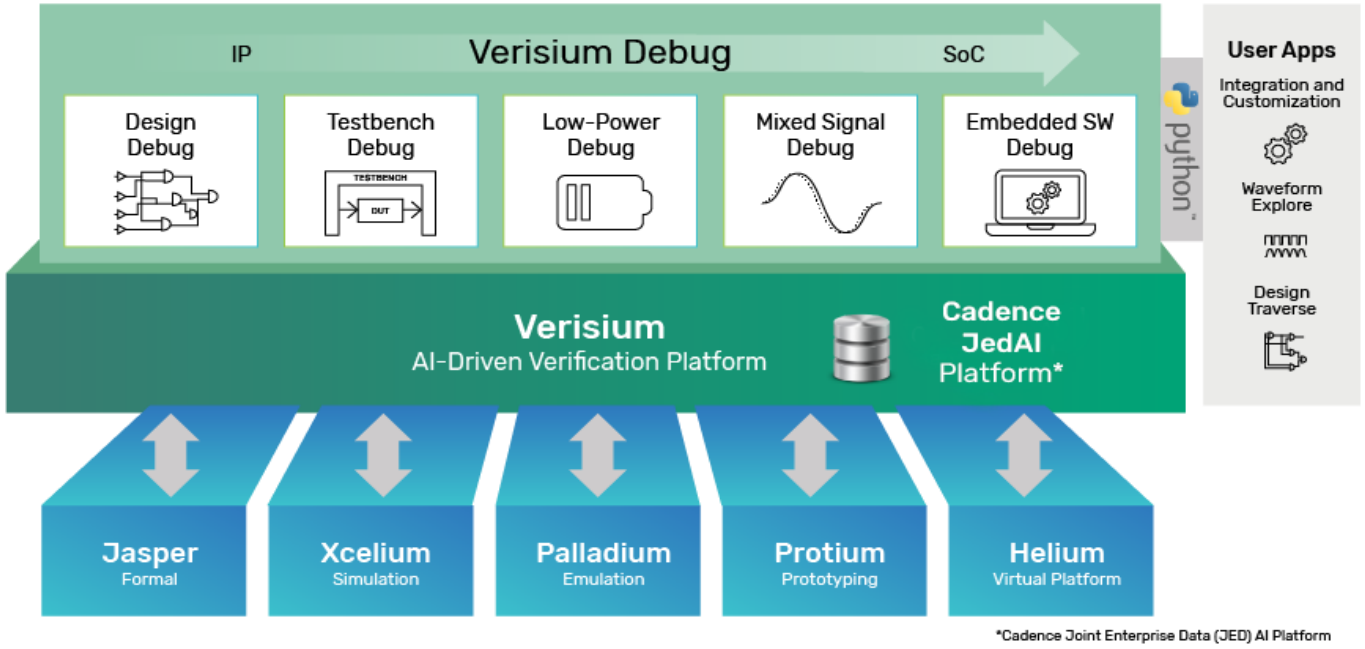


MS Verification debugging tools

- SimVision Mixed Signal Debug Option



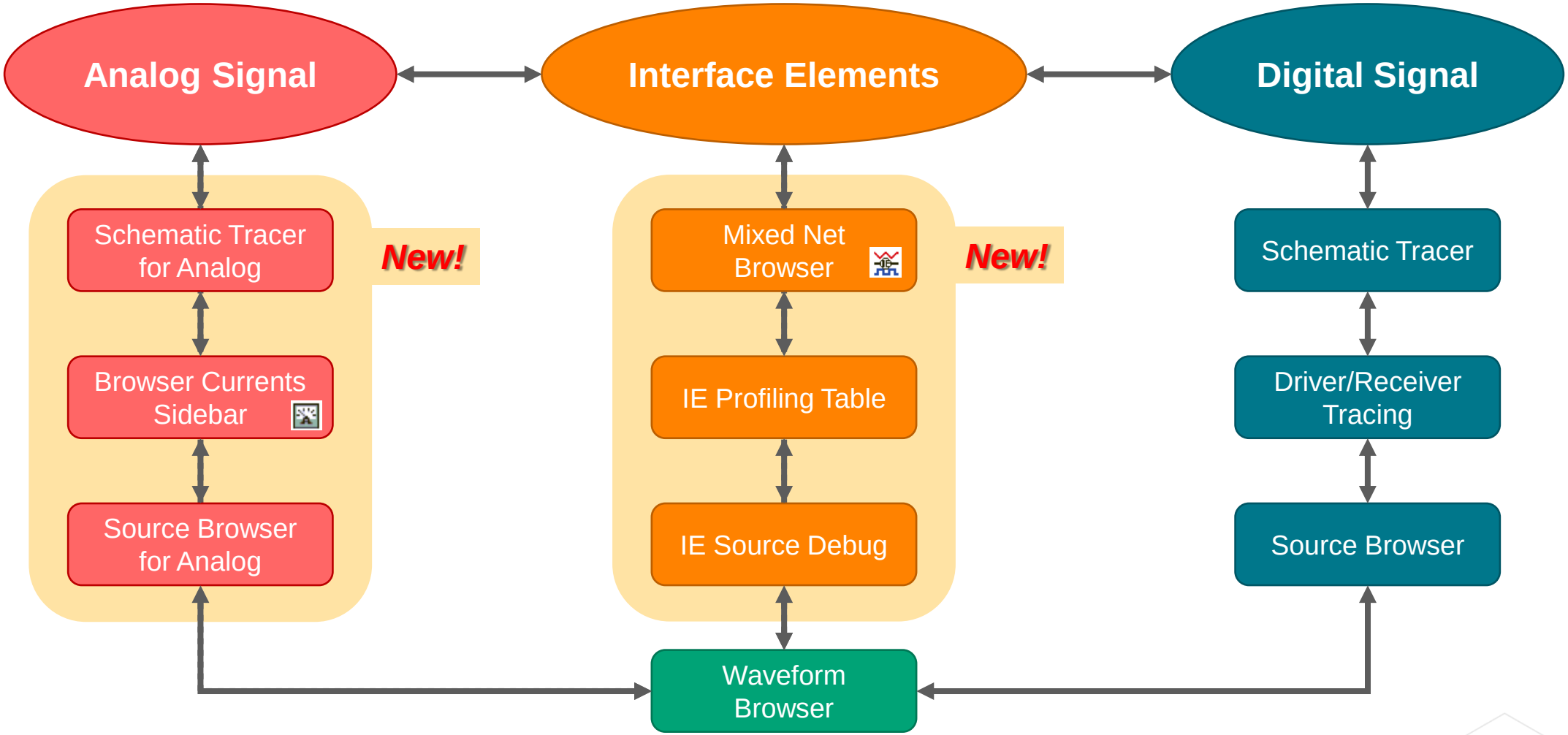
- Verisum Debug



*Cadence Joint Enterprise Data (JED) AI Platform

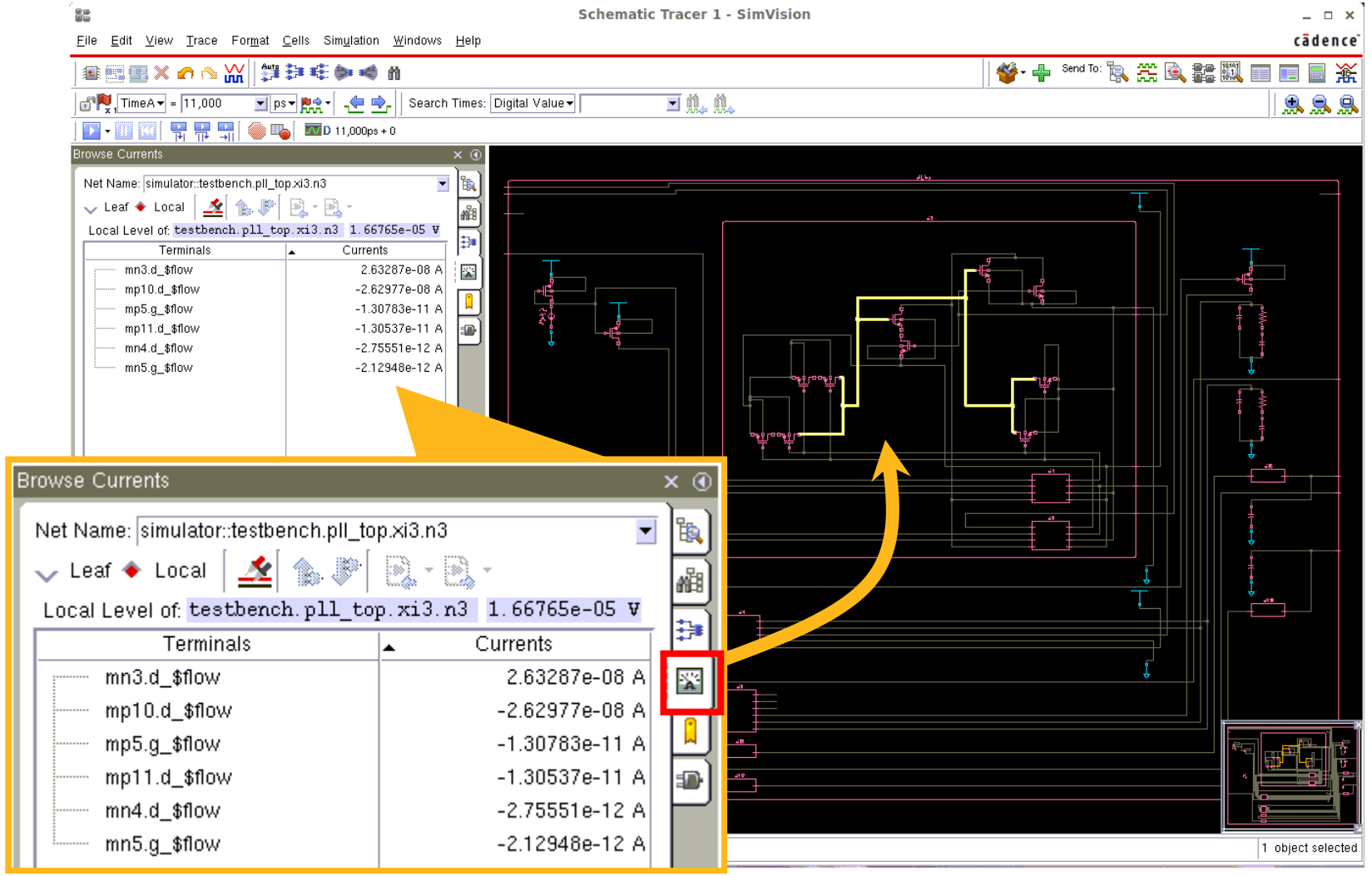
SimVisionMS Debugging Flow

When you find an issue in your design -- debugging starts from where the issue is found

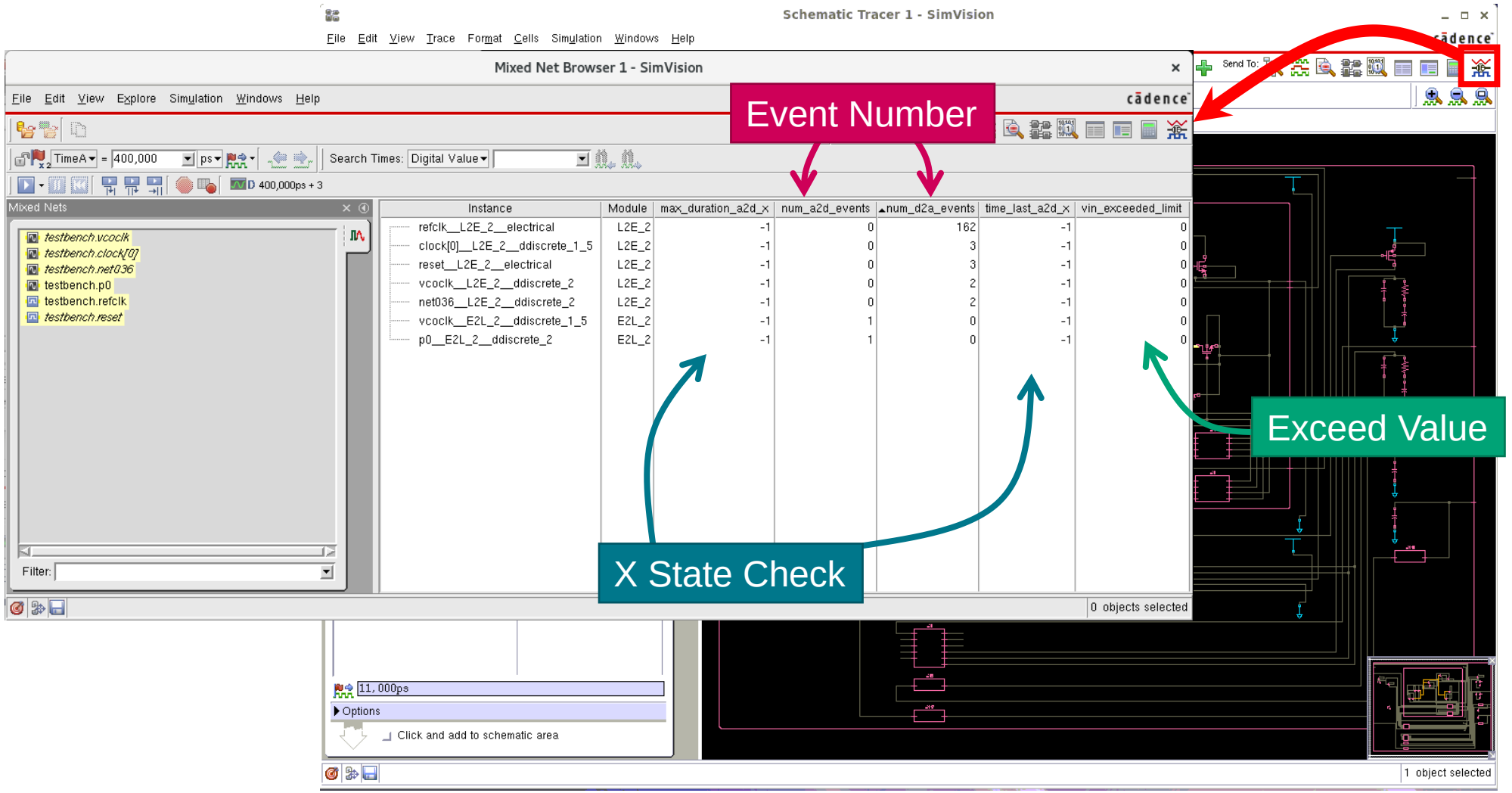


Interactive Browse Currents Tab in Schematic Tracer

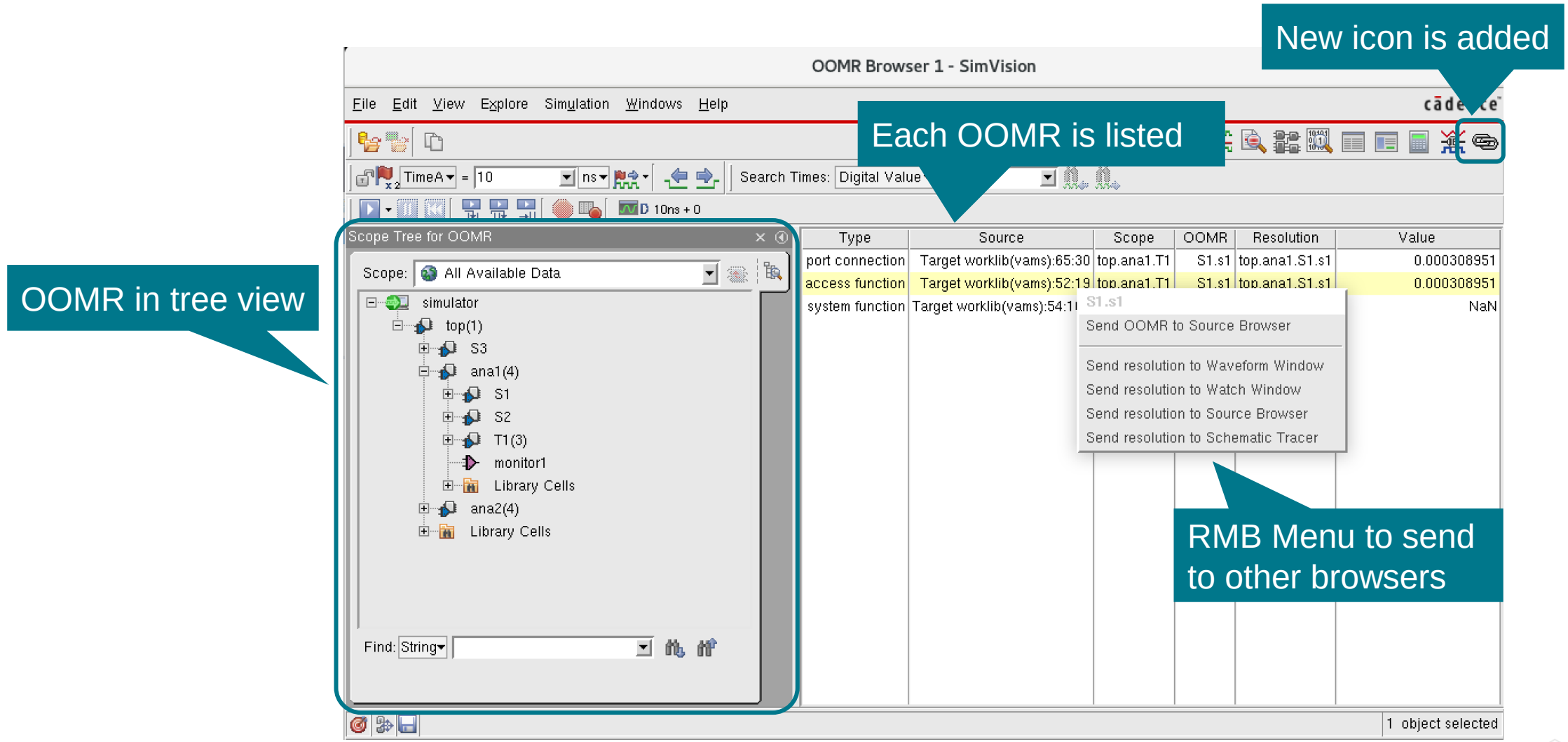
- Know the current flow value and direction



Mixed Signal Nets and IE/CMs Profiling in Mixed Net Browser



OOMR Browser GUI



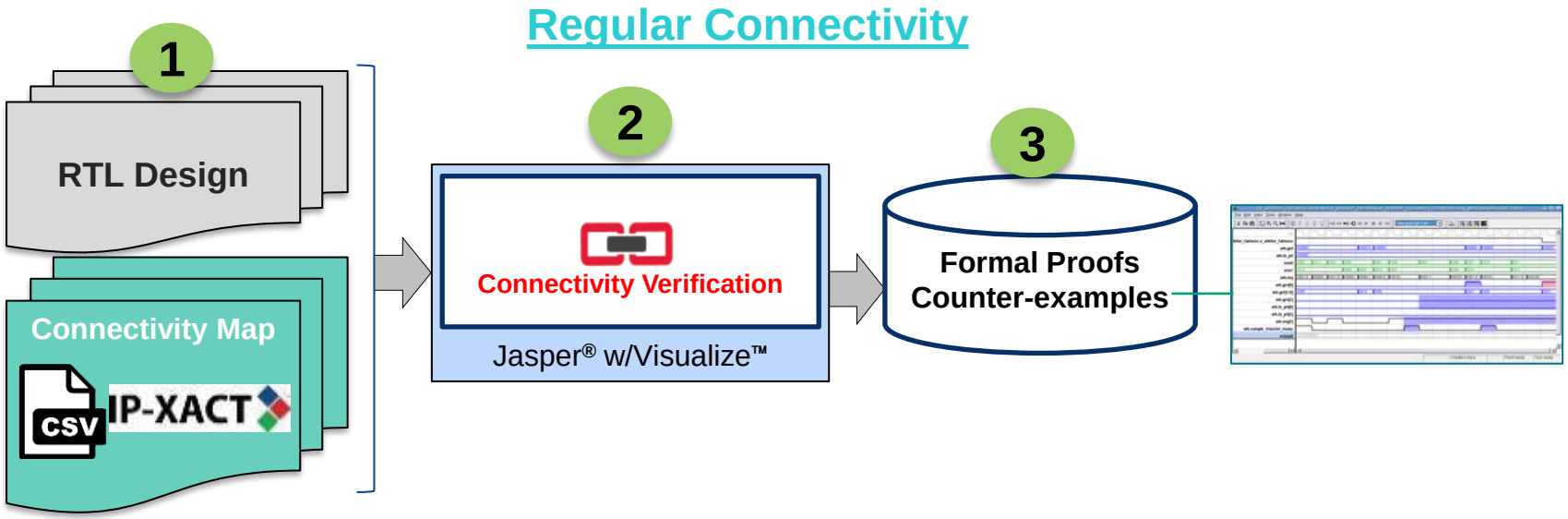
Cadence Mixed Signal Verification Innovations

RNM Leveraged from Simulation to Emulation

✓ Ability to emulate Real Number Models – Palladium Z3

- Verify analog behavior in larger Mixed Signal SoC
- Runtime Speed Up – **1000x** and within **0.1%** accuracy compared to simulation (XLM or Spectre)
- Robust System Verilog Language Support for Real Number Modeling RNM
  - Wreal, Real, System Verilog UDN (ex – EEnet)
- Allows Mixed Signal SoC verification of
  - Analog Trim
  - Analog Start Up
  - DSP <-> Analog interaction behavior modeling
  - PMC Control with RNM based Power Supply Models

Jasper Connectivity Flow



DMS Connectivity Enhancements

- Extend the support for Verilog AMS and SV-RNM files
- DMS types supported
  - `real (SV var) , wreal (VAMS net)`
  - `wreal1driver, wreal4state, wrealmin, wrealmax, wrealsum, wrealavg` (cds_rnm_pkg net with dedicated resolutions in VAMS and SV)
  - `EEnet` (EE_pkg types)
- Connectivity between scalar types real and logic can be proven
  - Real types are converted to a single bit logic type to enable connectivity checks
  - Complex type `EEnet` connectivity still requires the path to be all `EEnet` throughout the path

Xcelium Mixed-Signal Success Stories

Renesas: SVRNM / High-Performance DV MS Verification

Simulation results

- Complete comparison for 4 models. (rating: **high**, **medium**, low)

Winner for digital heavy simulation

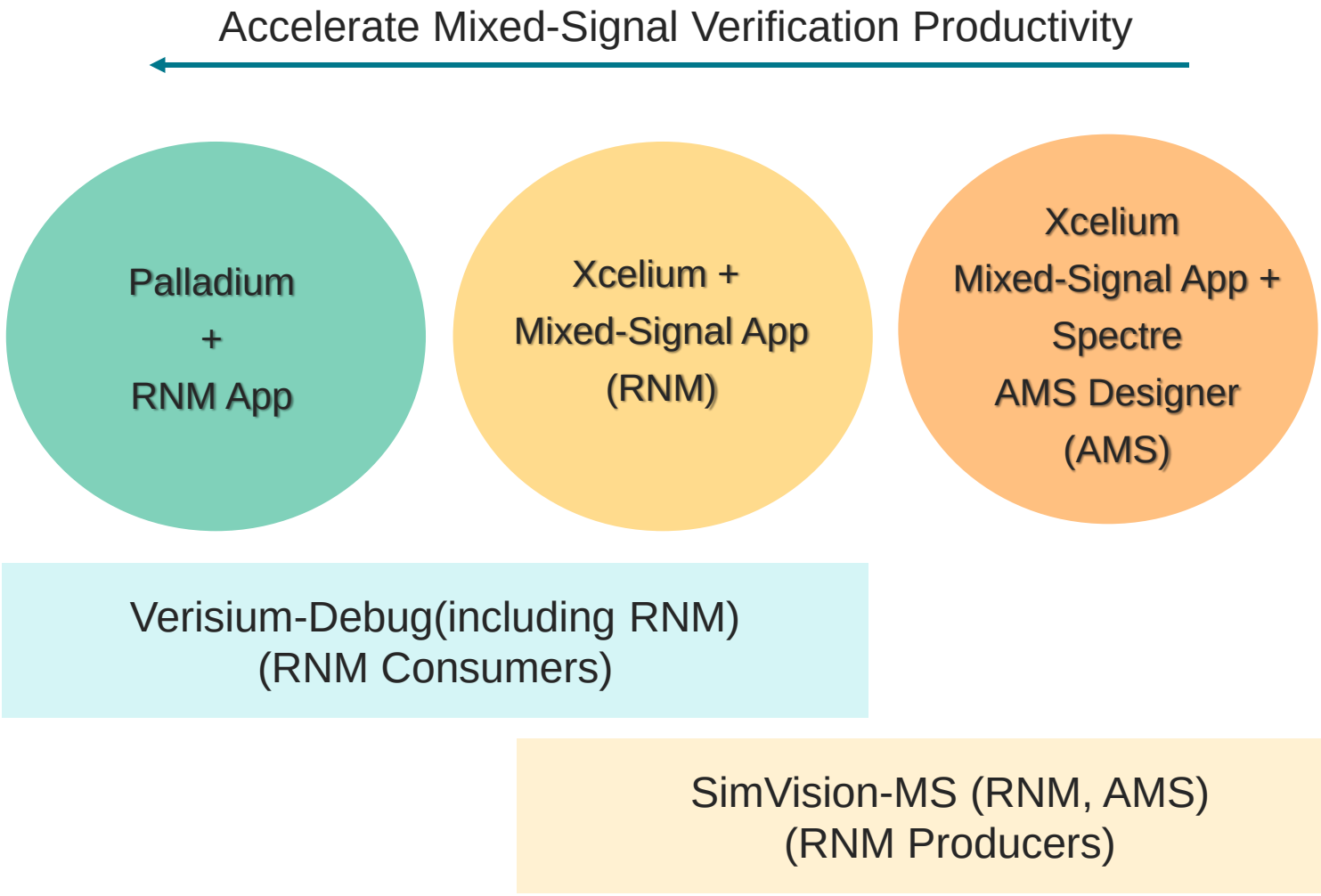
	AMS model	Open-loop RNM	Closed-loop RNM	Closed-loop RNM with EENet
Driver	AMS driver	Digital driver	Digital driver	Digital driver
Development difficulty	Difficult (deal with convergence issue and slow sim optimization)	Easy	Difficult (deal with mathematical equation)	Medium
Change to schematic	No change	Yes, combine all blocks into one model file	Yes, combine charge pump, loop filter.	No change
Accuracy	Highest	Lowest	High	High
Sim time in individual testbench	14 min (can be reduced based on optimization)	~1 second	~1 second	~1 second
Sim time in a top-level verification test: data path	Not tested	16 min 10 s	22 min 18s	21 min 35s

Note: Won the 2nd best paper award in DVCon 2023

2025 Cadence Mixed Signal Verification Vision

Mixed-Signal Verification Vision: 2025 and beyond

Accelerate verification productivity – across Mixed-Signal Simulation, Emulation and Debug



- Xcelium Mixed-Signal App
  - Build Performance (MSIE, Seamless DMS)
  - Runtime Profiling of SVRNM resolution
  - Native RNM/wreal Tran Engine
  - Verisium-Debug + DMS Enhancements
- EEnet Model Library
  - Rapid analog model development
    - (RNM simulation, emulation flow*)
  - Command line, Virtuoso support
- Accelerate RNM via Palladium
- MS Debug (Producers, Consumers)
- Model Validation (Stealth mode)
  - Simcompare for RNM, AMS regressions

Summary

Summary

For High Performance, High Quality, Seamless Mixed-Signal Verification

- Single mixed-signal elaboration and simulation solution for complex SoCs and multi-chip designs
  - Common MS simulator within *domain-specific* environments (DV, Analog)
  - Seamless use model in both command-line/DV and Virtuoso/Analog environments for highly productivity hand-off between DV and Analog
- Simulation planning, regression, and traceability using Verisium Manager™ Metric-Driven Signoff Platform
- Use with Virtuoso ADE Assembler and Verifier for simulation management and distribution with an analog point of view