TESSOLVE

A HERO ELECTRONIX VENTURE

Webinar 3: AI Assisted Advanced DV Flow & Use cases ✨

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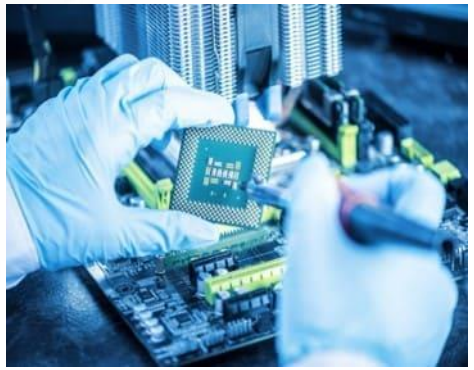
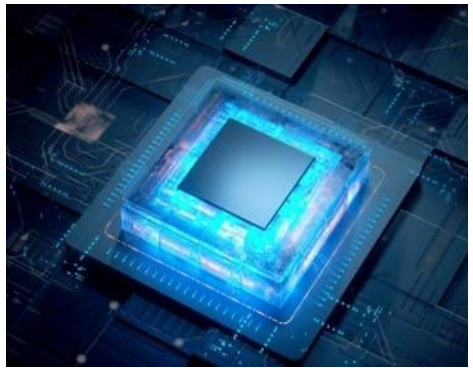
Chip Design



Test Engineering

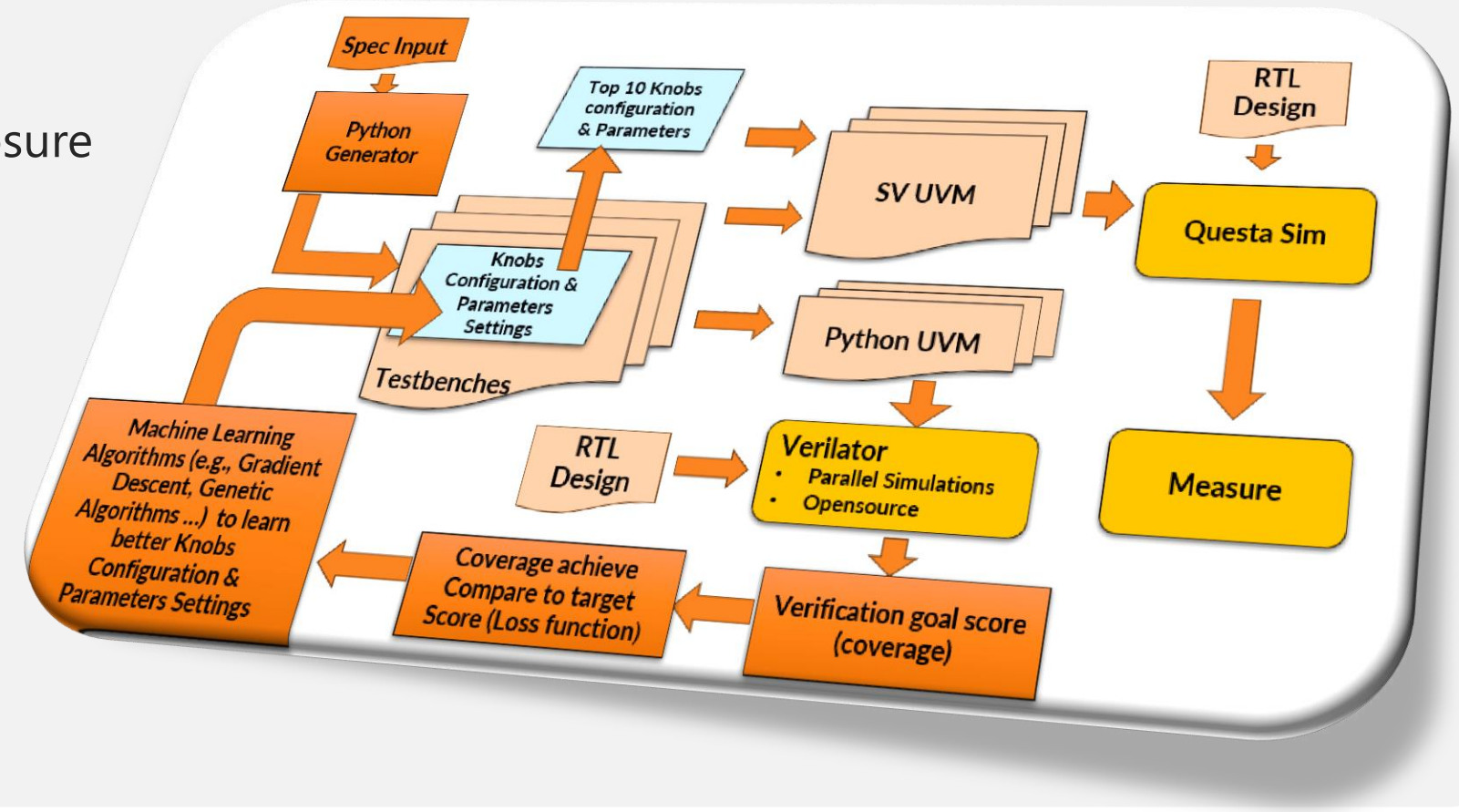
Hardware Design



Embedded Systems

Outline

- 1: UVM AI Training Tool
- 2: Basic TB Generation Tool
- 3: Automating Coverage Closure
- Collaboration Opportunity



AI Ecosystem

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Knowledge Bots:

- **Features:** Faster to develop & deploy
- **Use case:** With less confidential data, Project CoPilot
- **Security:** Low
- **Cost**: Low
- Reasonable accuracy,
- **Project:** UVM Chatbot, FUSA Chatbot

Build: Cloud Deploy: Cloud/ Hosting Services

- **Feature:** Faster develop & deploy
- **Use case:** Client projects, highly confidential data.
- **Security:** High
- **Cost**: High

Build: Local Deploy: Local

- **Features**: Slower to develop & slower to deploy
- **Use case:** For highly confidential data
- **Security:** High
- **Cost:** High
- **Challenge:** Less Adaptability, less Scalability, Upfront Cost

AI-Auto Agents / Apps

- DV Spec Extraction Tool
- UVM TB Automation
- Assertify tool
- AI code copilots
- AI Training Tools, FUSA, PDK, **UVM** etc.
- **Basic TB Generator**
- **Automating Coverage Closure**

AI/ML Experiments in IP Verification

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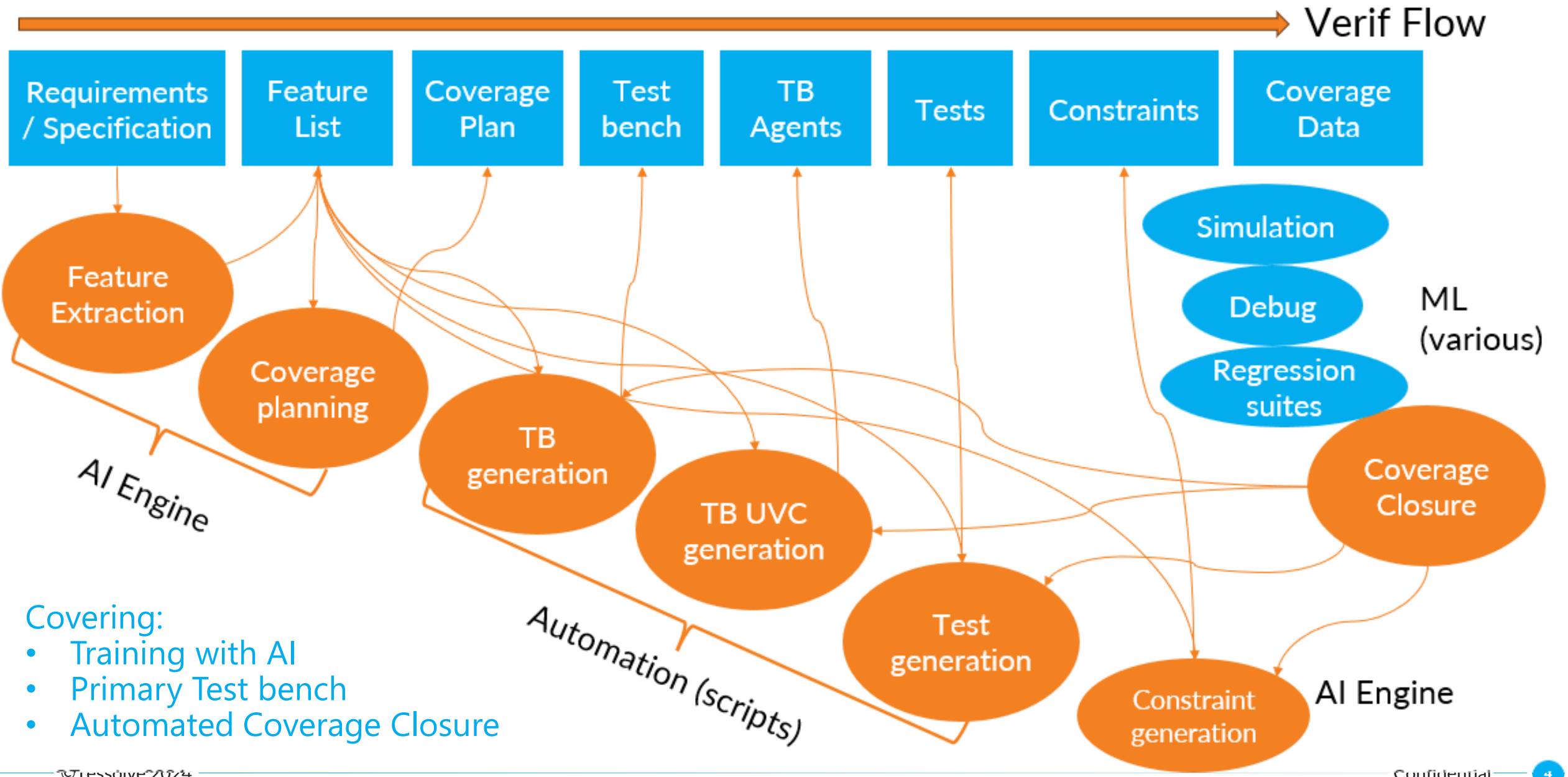

Covering:

- Training with AI
- Primary Test bench
- Automated Coverage Closure

1: UVM AI Training Tool

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Organized Content
- Follows planned flow

Quick Topics
- Most important topics' explanation

MCQs
- Test, Evaluation, weak concept suggestions

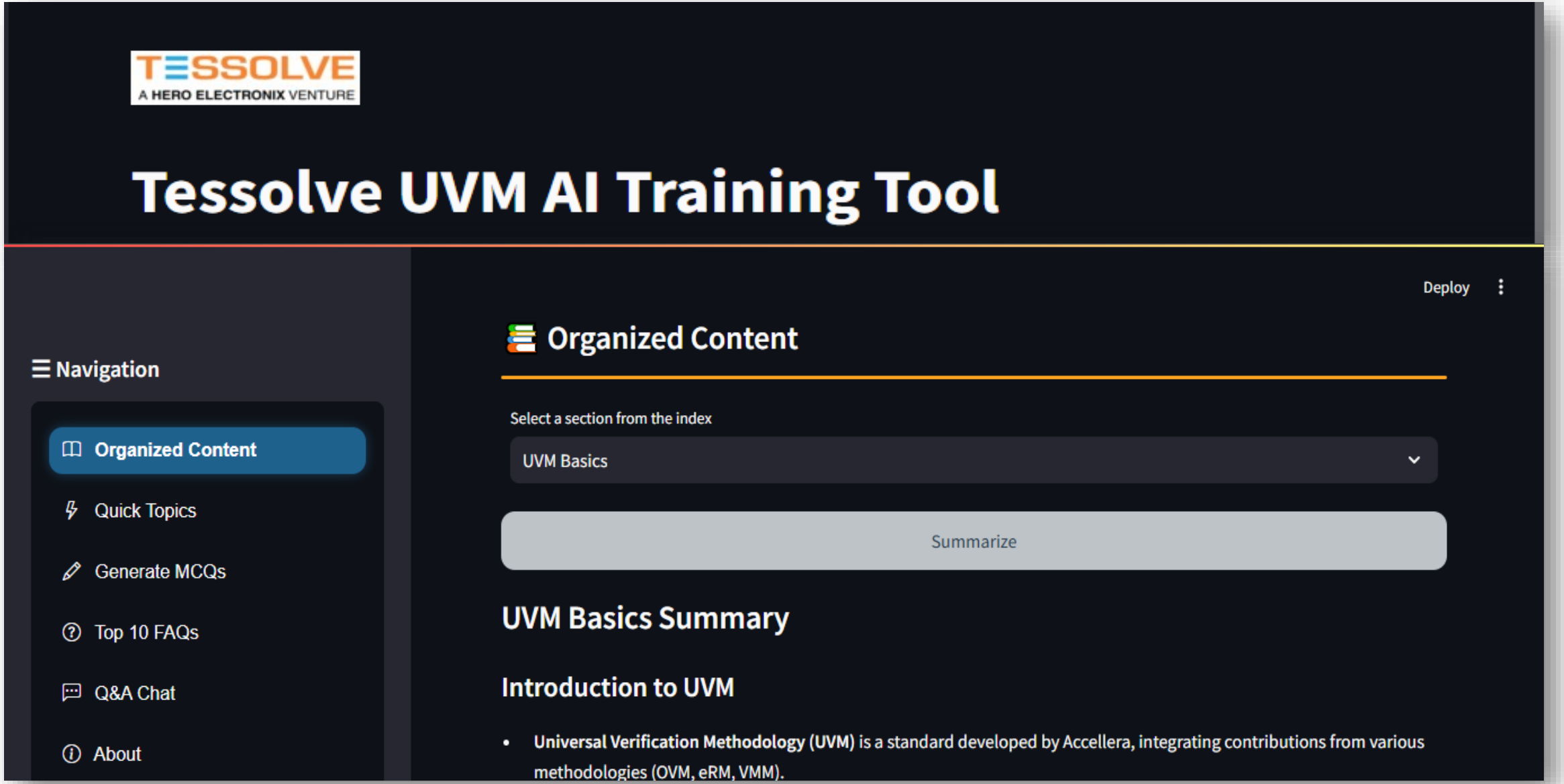
FAQs
- Clarifies on common important doubts

Q&A
- ANY question support

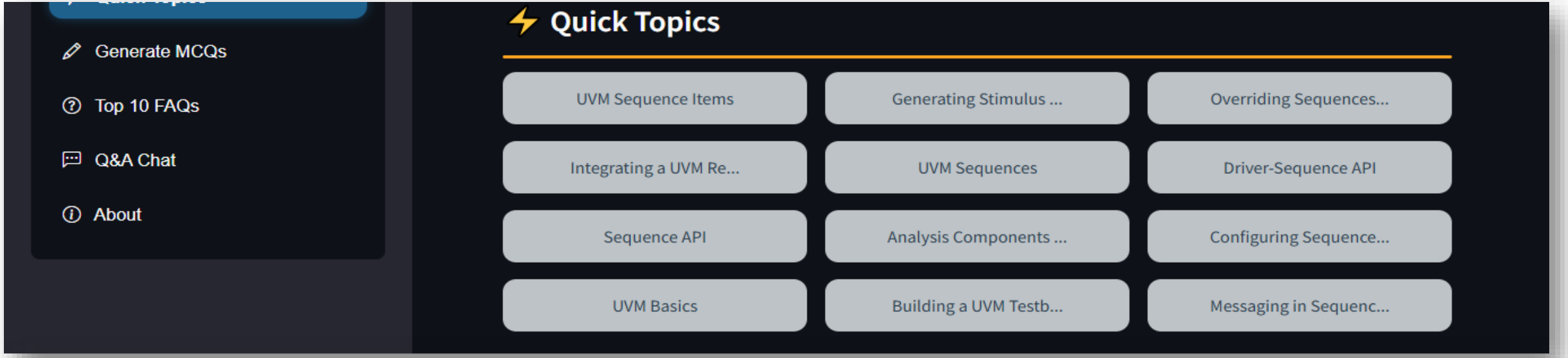
About
- Tool briefing for effective use

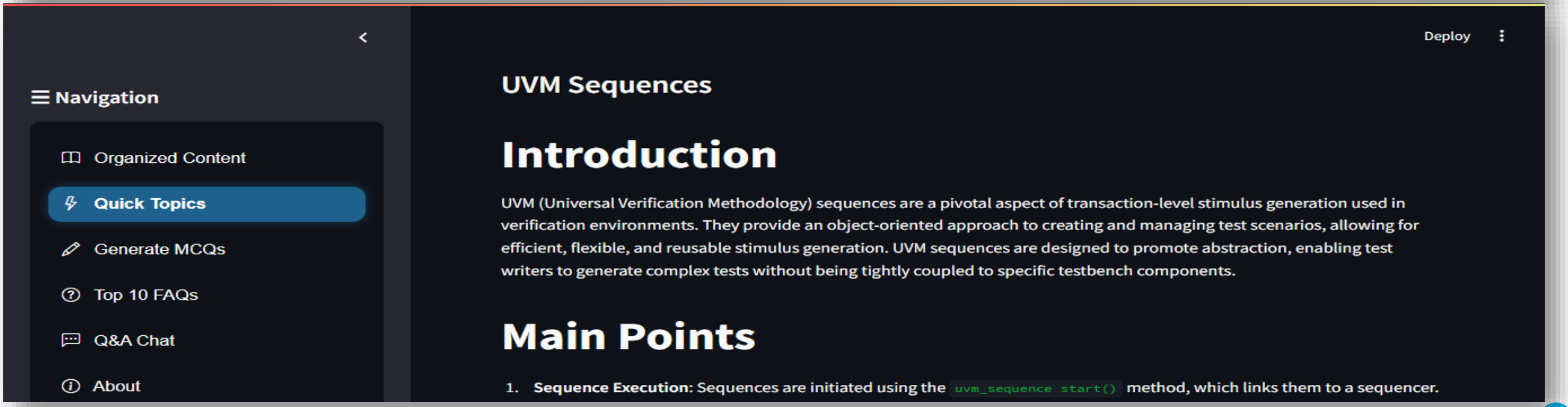
Benefits:
- Self guided and self paced flow
- Analytics & custom topic suggestions
- Ask anything about UVM
- Improved accessibility
- Reduced training time
- Scalable for other domains

1: UVM AI Training Tool

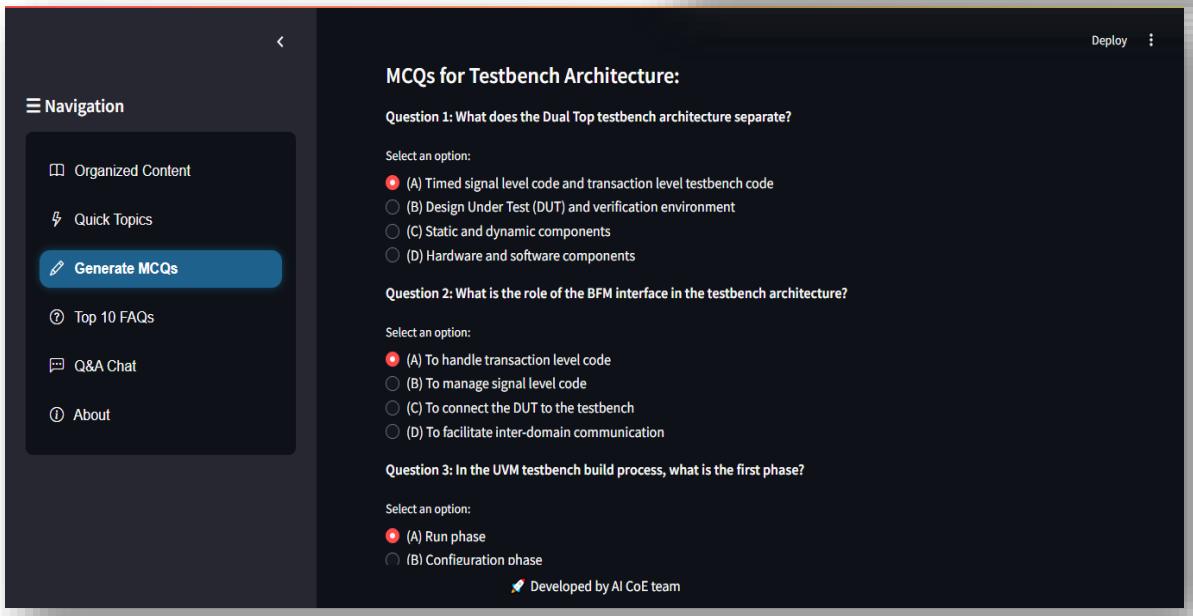


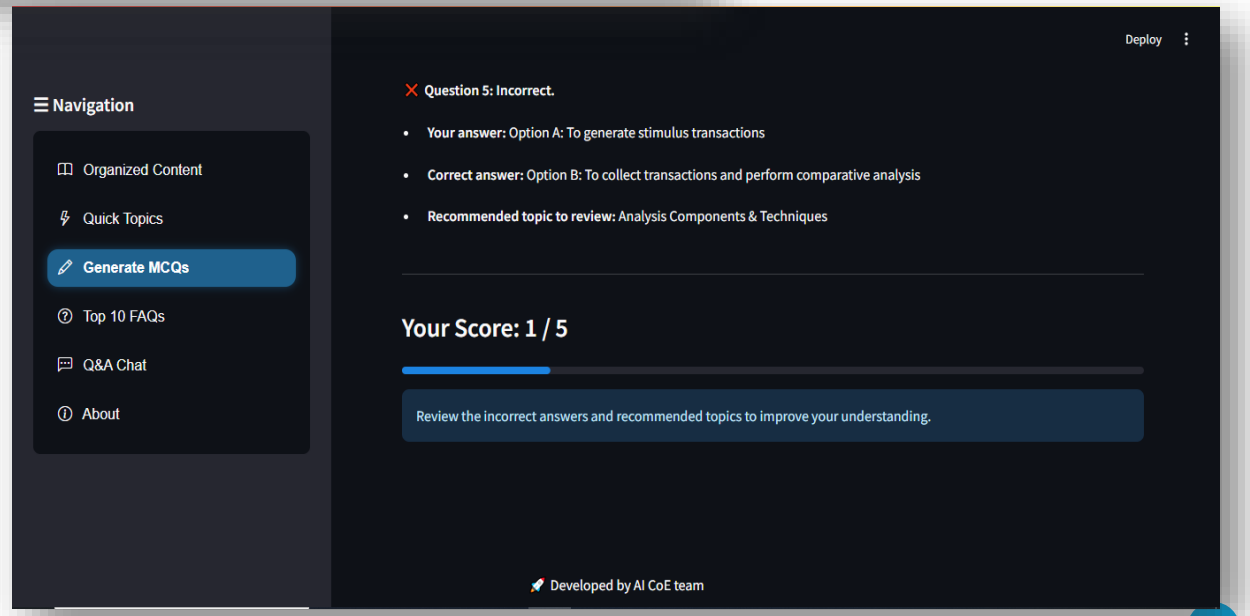
1: UVM AI Training Tool





1: UVM AI Training Tool





2: Simple TB Generation – Independent Verification for Designers

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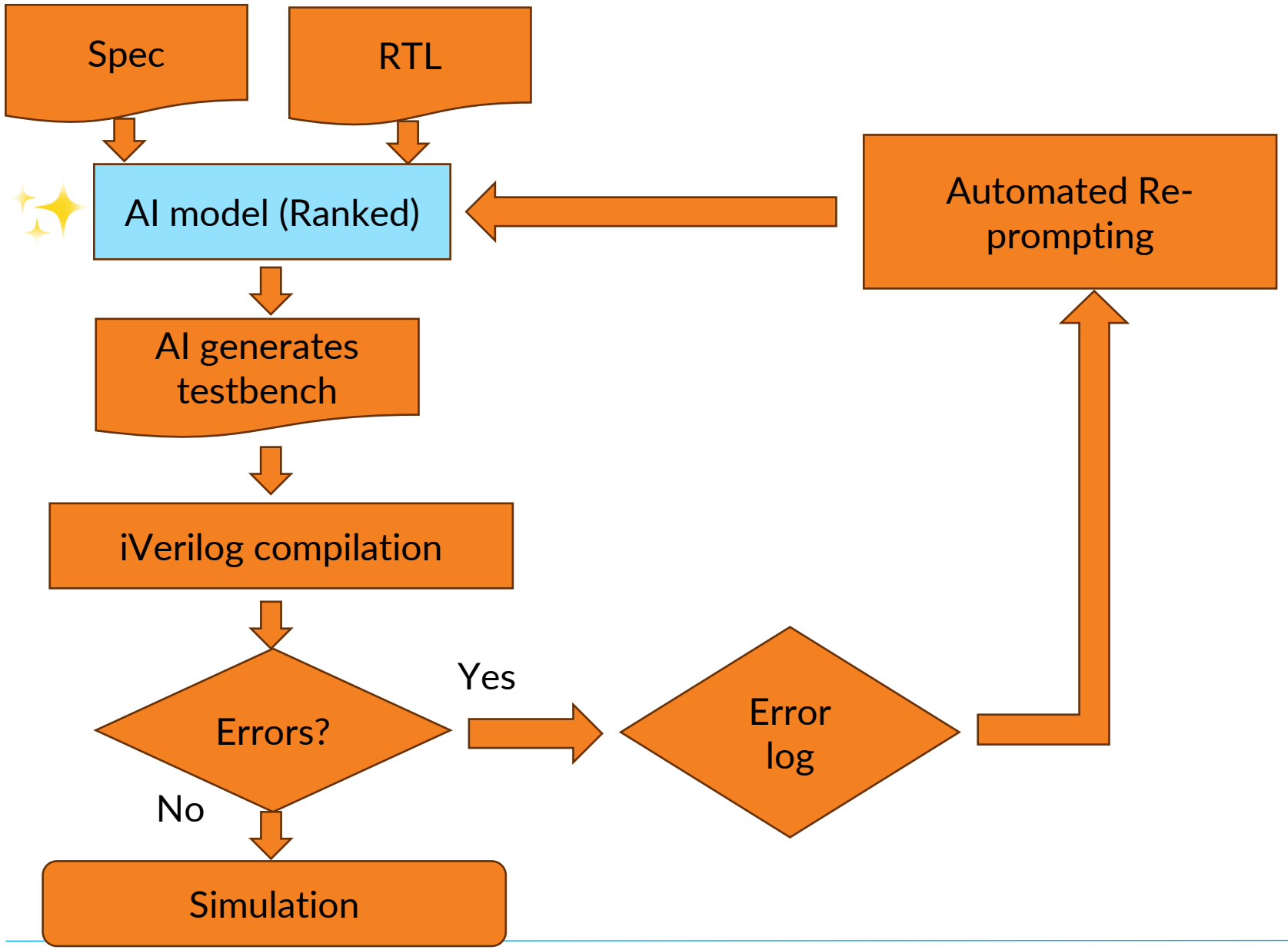
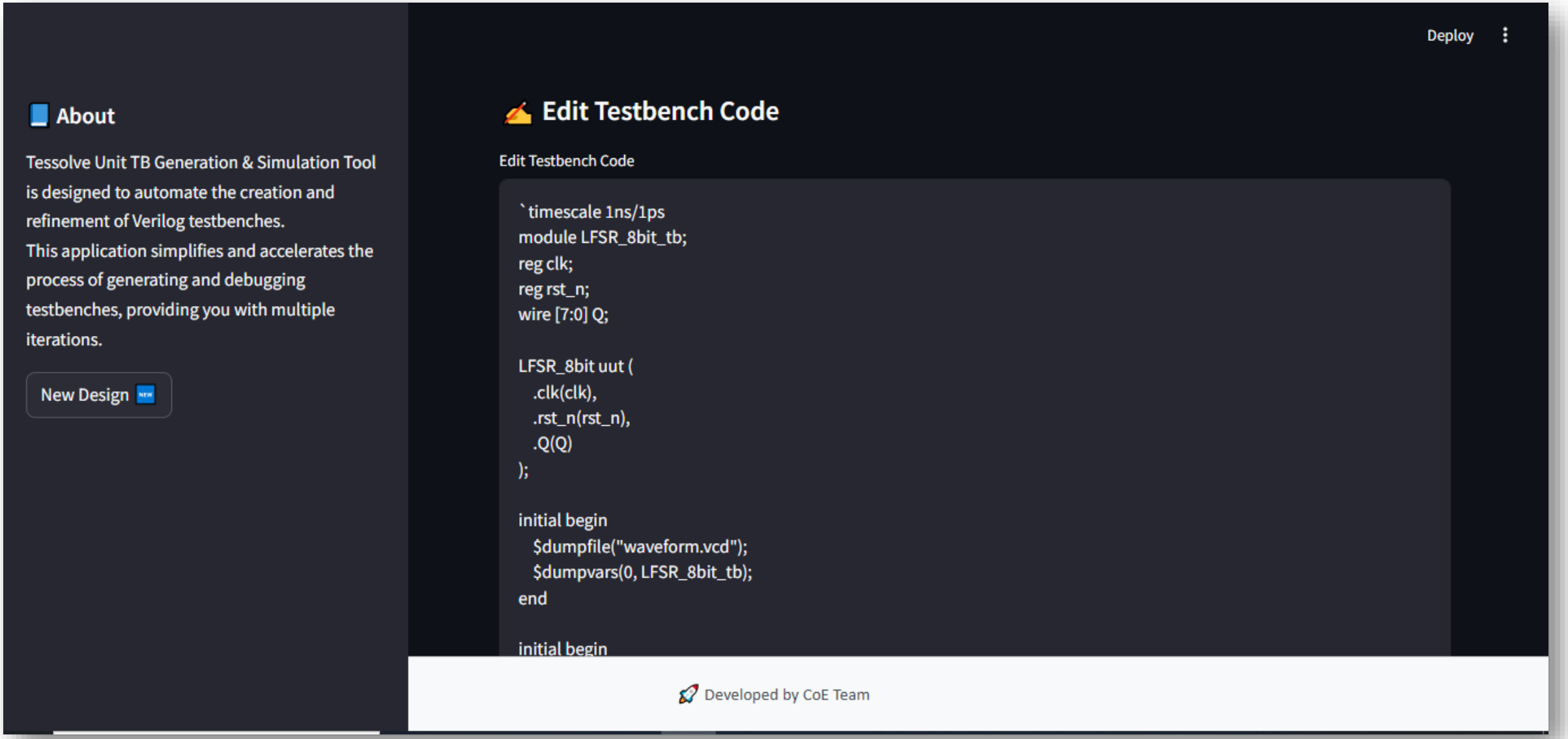
- There is always a need for designers to have a basic test bench to make sure the RTL is basically functional before handing it to verification.
- But there is a concern for independence otherwise designers are just verifying their understanding – a single point of failure.
- We demonstrate our tooling that can generate simple test bench from the specification either in Verilog or SV
    - if preferred by the designer
    - or basic UVM if they prefer
- Designers can add “designer knowledge” to their generated test bench
    - For example:
        - Assertions
        - functional coverage
        - A scoreboard function (test bench hooks can be given for that)
    - Verification engineers can decide if they want to reuse them
        - With full knowledge of any associated risks

2: Simple TB Generation Tool



2: Simple TB Generation Tool



2: Simple TB Generation Tool

2: Simple TB Generation Tool

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A quick first cut basic SV testbench generation tool to help designers to get easy debug of the RTL.

Features:

- AI TB generation
- Error feedback
- Tool chain Integration for compilation, simulation

Benefits:

- Error handling
- Accelerate designer “smoke test” verification
  - No need to involve DV
- Time saving
- Tool integration saves lot of time
- Opensource tool set

3: Automating Coverage Closure – The Ultimate Objective

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Achieving coverage closure in verification is challenging, consuming up to 80% of efforts. Automation in this area remains a formidable challenge. Tessolve leverages AI to automate this process effectively.

Benefits:

- Reduced verification efforts
- Fast opensource simulation
- High efficiency feedback loop
- Complete automation

Python UVM Test Bench Generation:

- Generation of test bench with numerous "knobs and hooks" to configure the constrained random generation.

Intelligent AI agents:

- By intelligent AI agents and employing a suitable loss function, we guide the system towards the coverage goal.

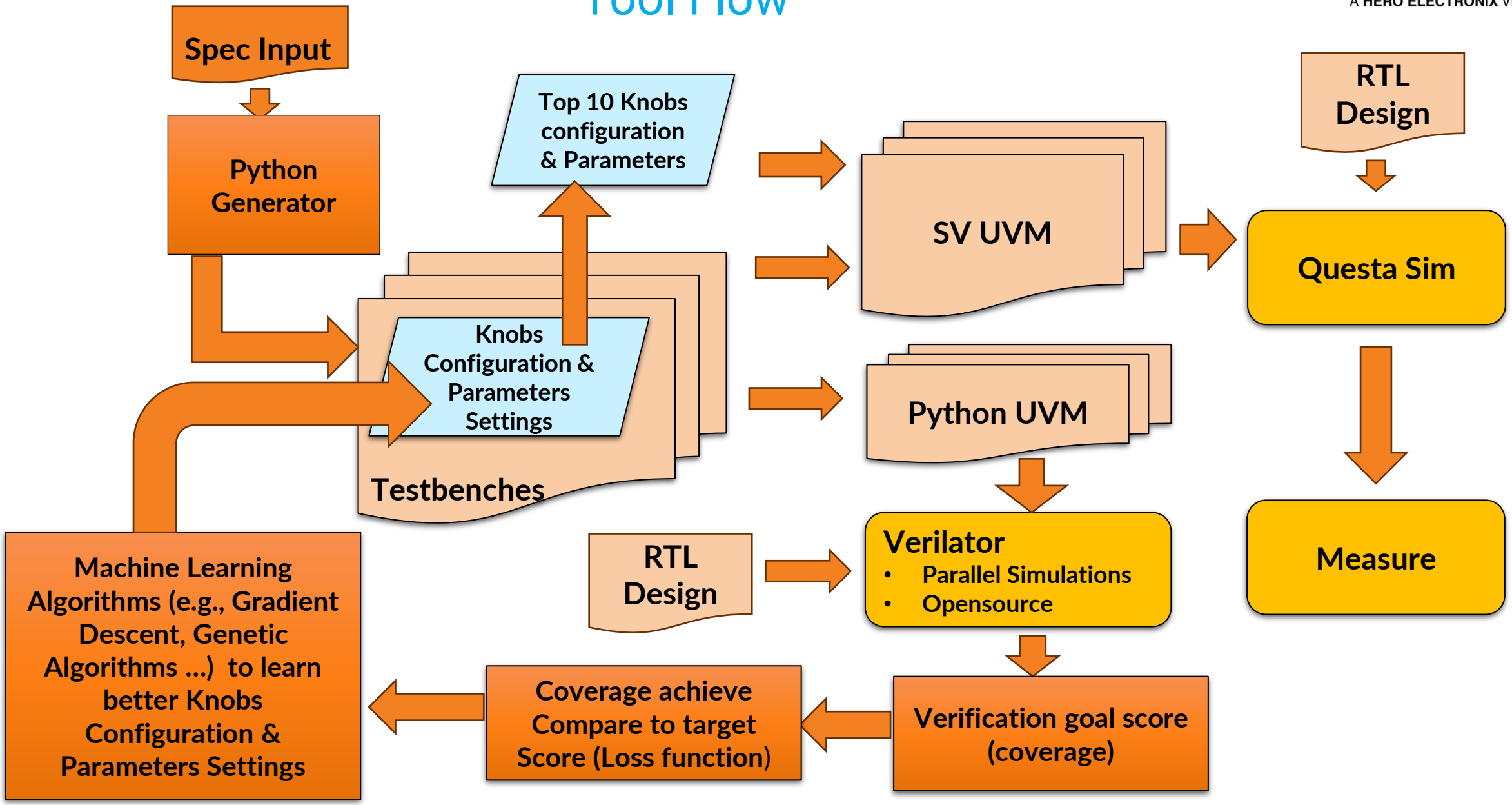
Machine Learning Techniques:

- Techniques such as gradient descent or genetic algorithms are employed by ML to achieve the desired coverage.

Simulation Strategy:

- Multiple simulations are crucial for the ML model to learn effectively. We demonstrate the use of a Python test bench with Verilator for quick, cost-effective simulations before transitioning to System Verilog (SV) with a recognized simulator for signoff. This approach helps mitigate the risk of different randomization outcomes.

Tool Flow


Spec Input
Python Generator
Top 10 Knobs configuration & Parameters
Knobs Configuration & Parameters Settings
Testbenches
SV UVM
Python UVM
RTL Design
Questa Sim
Measure
RTL Design
Verilator
• Parallel Simulations
• Opensource
Verification goal score (coverage)
Coverage achieve Compare to target Score (Loss function)
Machine Learning Algorithms (e.g., Gradient Descent, Genetic Algorithms ...) to learn better Knobs Configuration & Parameters Settings

Why Python for TB Generation?

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- We can still generate better test benches compared to AI
  - Re-use of previous generation via config files per design
    - E.g. re-use of previous test bench structures such as complex scoreboards
  - Python knows the split between static and dynamic UVM structures
  - Richer set of “knobs, config, and parameters”
    - All collected in a separate file to help the ML learning process
- But under constant review and adding specific AI solutions
  - Add AI for assertion generation
  - And functional coverage generation

Collaboration with DV Flow

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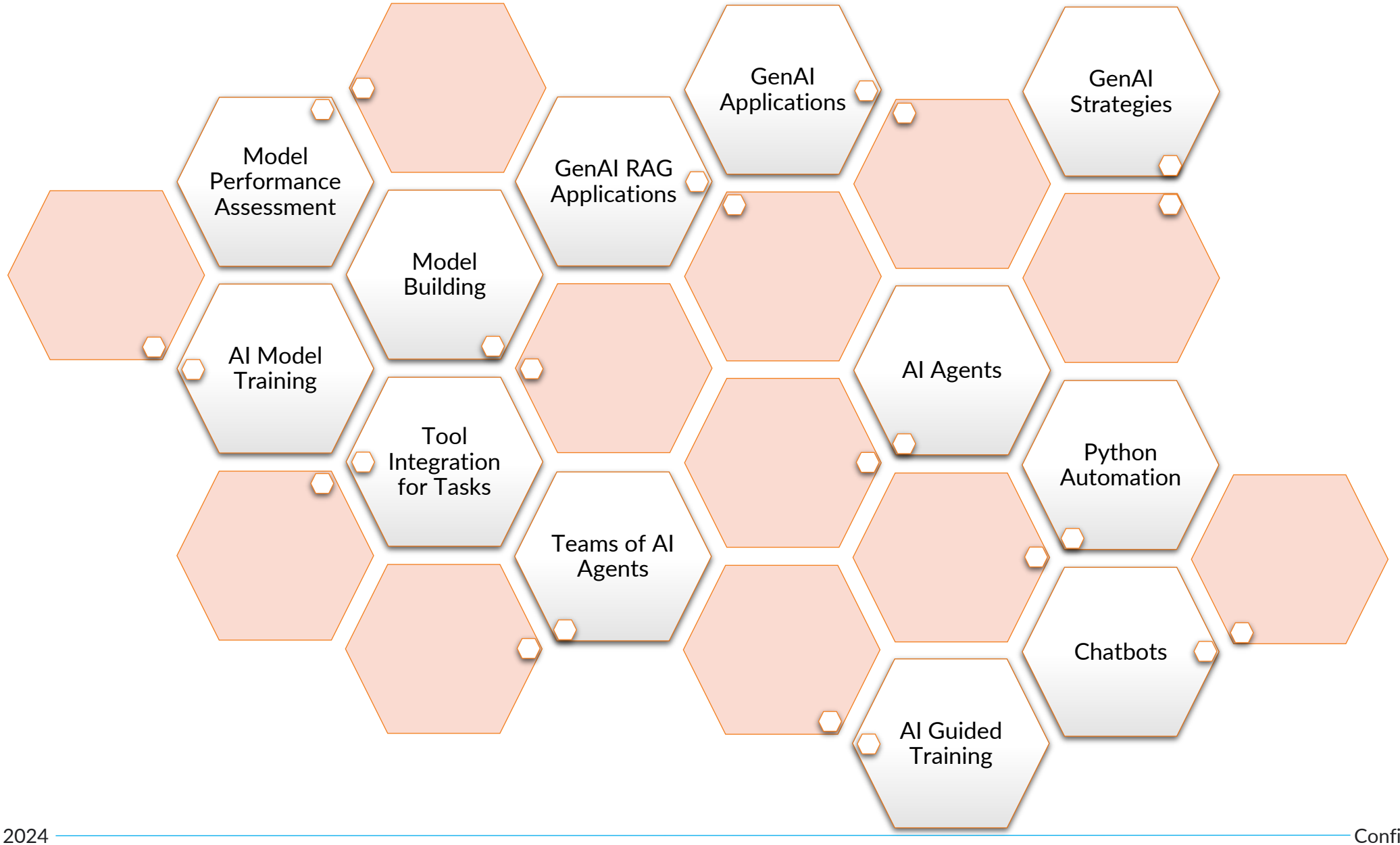
- Register Extraction
- Test Plan Generation
- Testcases
- Specification Analysis
- Coverage Planning
- Assertions
- Cover points
- Testbench Automation
- Feature Description
- Unit Test Bench Generation
- AI Agents for Tasks
- Tool Integration & Automated Validation

Collaboration with AI Research



Webinar Series Summary

Webinar 1 Registration	
Remote Access	230
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Companies	110

Webinar 2 Registration	
Remote Access	216
Countries	35
Companies	105

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THANK YOU

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Test Engineering

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