

TESSOLVE

A HERO ELECTRONIX VENTURE



Webinar 3: AI Assisted Advanced DV Flow & Use cases ✨

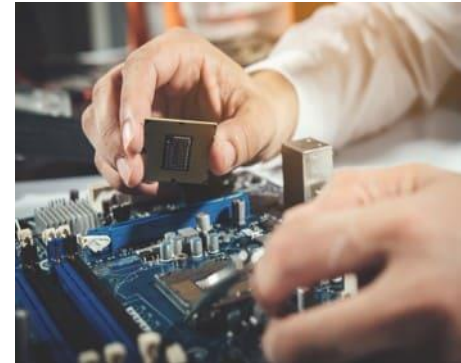
Mike Bartley, SVP, CoE | Marmik Soni, Sr. Design Lead, CoE



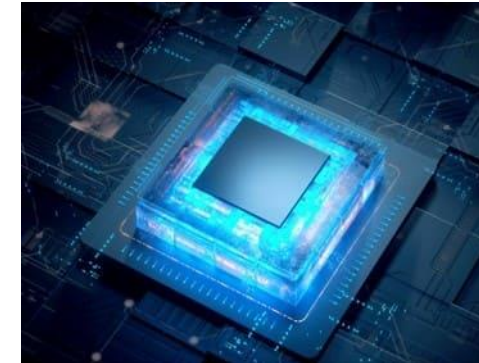
Chip Design



Test Engineering

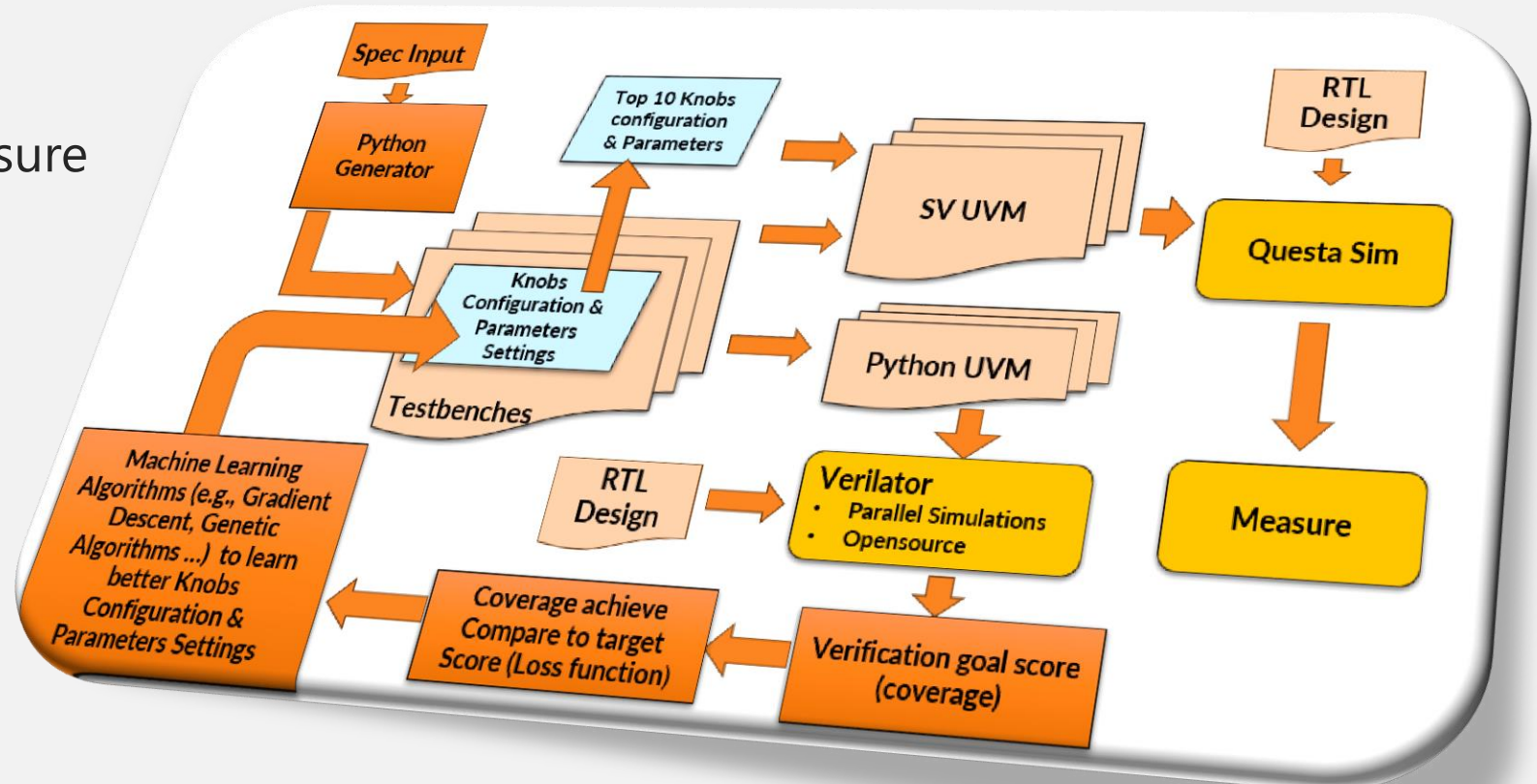


Hardware Design



Embedded Systems

- 1: UVM AI Training Tool
- 2: Basic TB Generation Tool
- 3: Automating Coverage Closure
- Collaboration Opportunity



Knowledge Bots:

- **Features:** Faster to develop & deploy
- **Use case:** With less confidential data, Project CoPilot
- **Security:** Low
- **Cost:** Low
- Reasonable accuracy,
- **Project:** UVM Chatbot, FUSA Chatbot

Build: Cloud Deploy: Cloud/ Hosting Services

- **Feature:** Faster develop & deploy
- **Use case:** Client projects, highly confidential data.
- **Security:** High
- **Cost:** High

Build: Local Deploy: Local

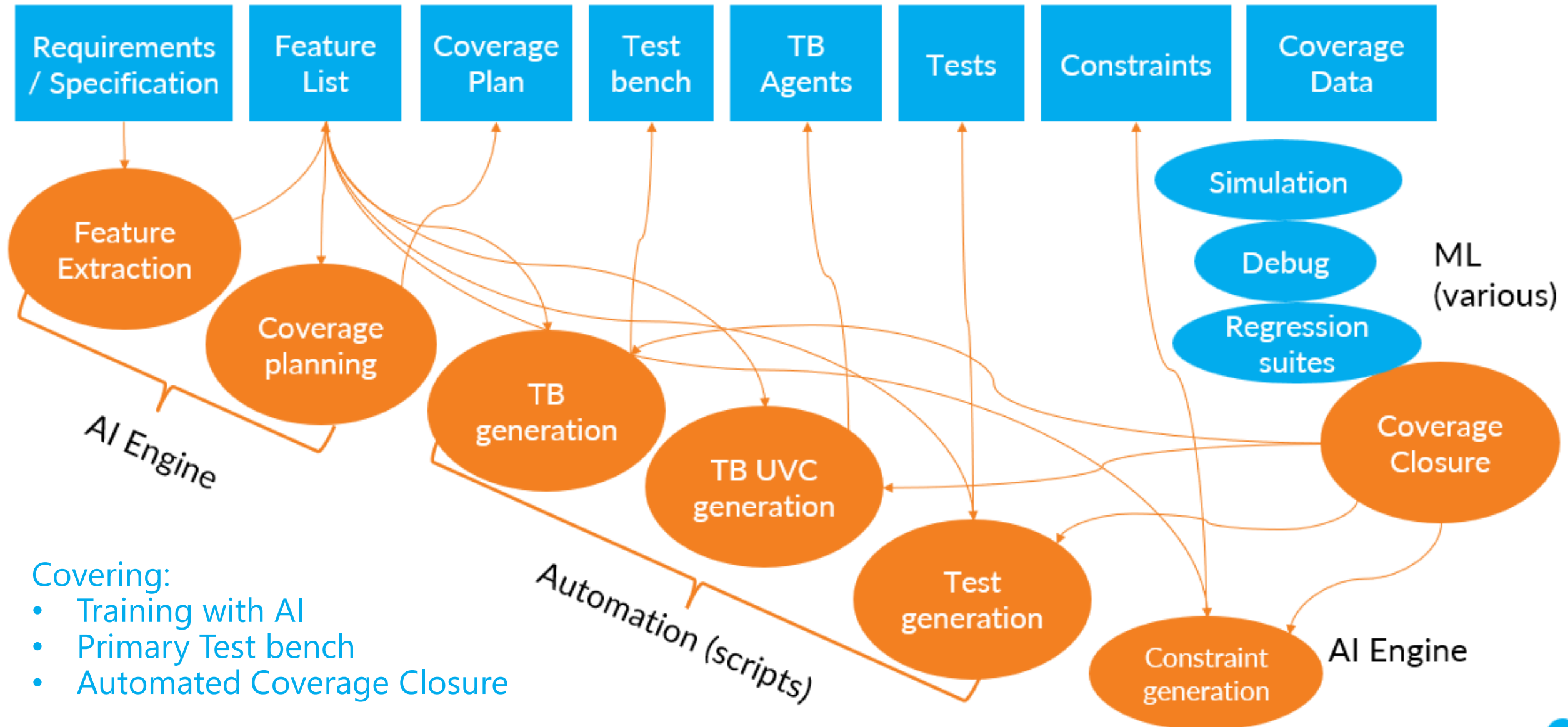
- **Features:** Slower to develop & slower to deploy
- **Use case:** For highly confidential data
- **Security:** High
- **Cost:** High
- **Challenge:** Less Adaptability, less Scalability, Upfront Cost

AI-Auto Agents / Apps

- DV Spec Extraction Tool
- UVM TB Automation
- Assertify tool
- AI code copilots
- AI Training Tools, FUSA, PDK, UVM etc.
- **Basic TB Generator**
- **Automating Coverage Closure**

AI/ML Experiments in IP Verification

Verif Flow



Covering:

- Training with AI
- Primary Test bench
- Automated Coverage Closure

1: UVM AI Training Tool

Organized Content

- Follows planned flow

Quick Topics

- Most important topics' explanation

MCQs

- Test, Evaluation, weak concept suggestions

FAQs

- Clarifies on common important doubts

Q&A

- ANY question support

About

- Tool briefing for effective use

Benefits:

- Self guided and self paced flow
- Analytics & custom topic suggestions
- Ask anything about UVM
- Improved accessibility
- Reduced training time
- Scalable for other domains

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Tessolve UVM AI Training Tool

Deploy

Organized Content

Select a section from the index

UVM Basics

Summarize

UVM Basics Summary

Introduction to UVM

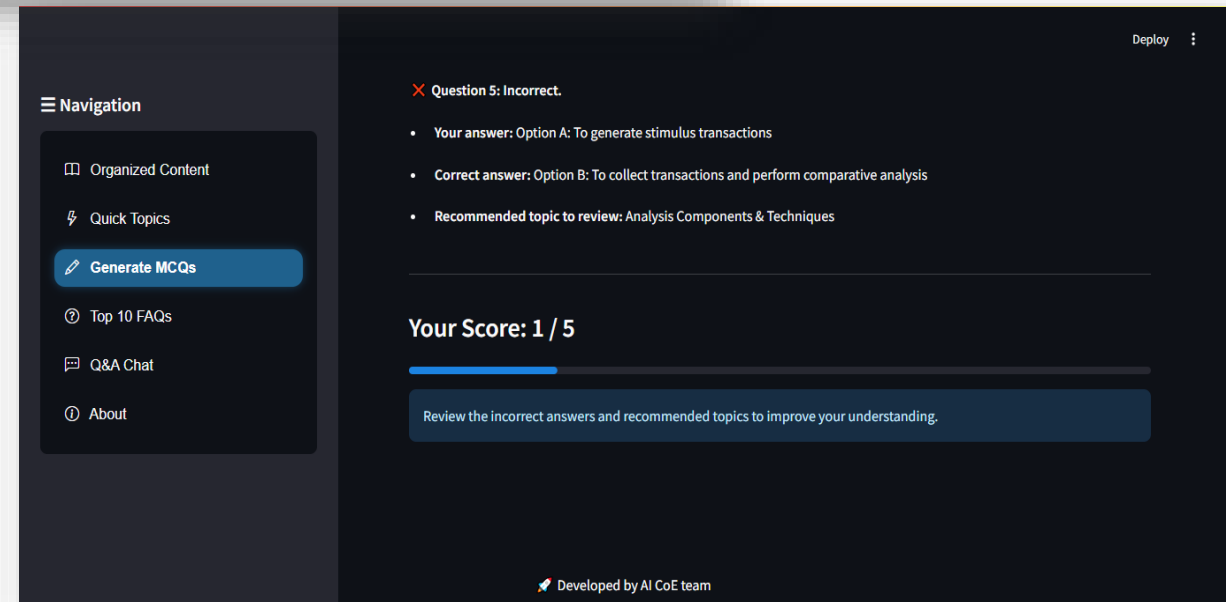
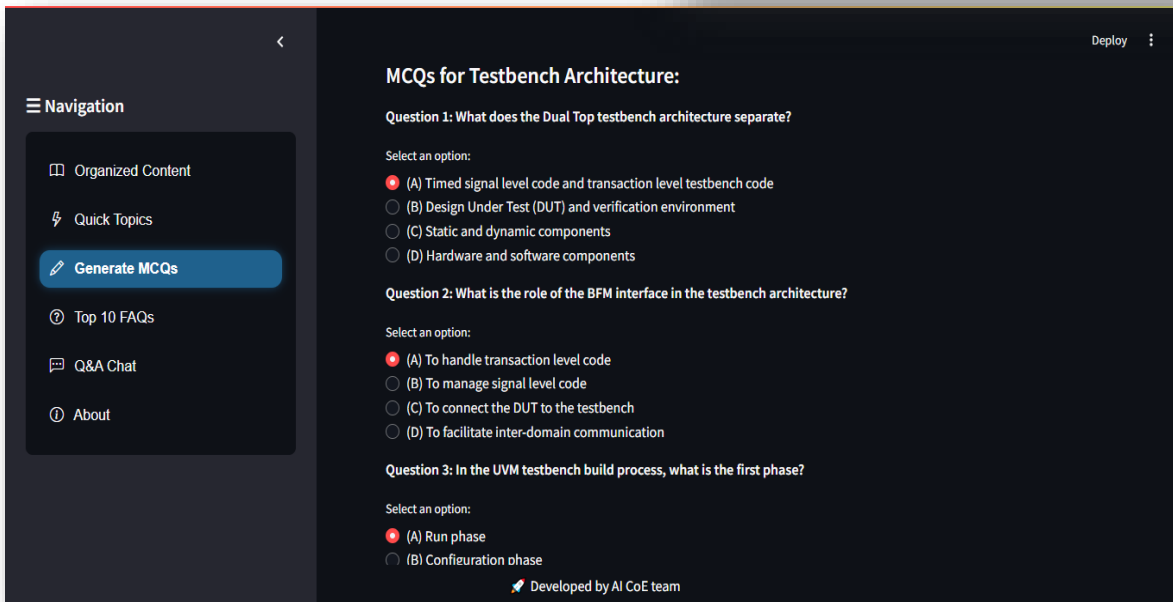
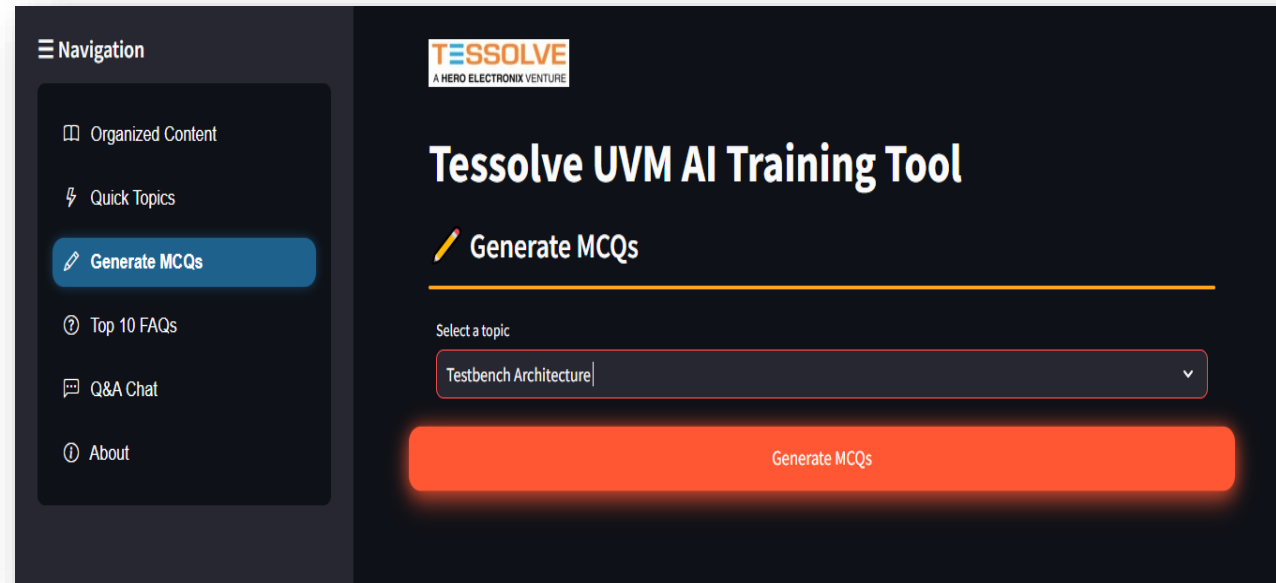
- **Universal Verification Methodology (UVM)** is a standard developed by Accellera, integrating contributions from various methodologies (OVM, eRM, VMM).

1: UVM AI Training Tool

The screenshot shows the top portion of the UVM AI Training Tool. On the left is a dark sidebar with a blue header bar. Below the header, there are four menu items: 'Generate MCQs' (with a pencil icon), 'Top 10 FAQs' (with a question mark icon), 'Q&A Chat' (with a speech bubble icon), and 'About' (with an information icon). The main content area has a dark background with a yellow lightning bolt icon and the text 'Quick Topics' at the top. Below this is a grid of 12 light gray buttons arranged in 4 rows and 3 columns. The buttons contain the following text: Row 1: 'UVM Sequence Items', 'Generating Stimulus ...', 'Overriding Sequences...'; Row 2: 'Integrating a UVM Re...', 'UVM Sequences', 'Driver-Sequence API'; Row 3: 'Sequence API', 'Analysis Components ...', 'Configuring Sequence...'; Row 4: 'UVM Basics', 'Building a UVM Testb...', 'Messaging in Sequenc...'

The screenshot shows the bottom portion of the UVM AI Training Tool. The sidebar on the left is dark with a blue header bar containing a hamburger menu icon and the text 'Navigation'. Below the header are five menu items: 'Organized Content' (with a folder icon), 'Quick Topics' (with a lightning bolt icon and highlighted in blue), 'Generate MCQs' (with a pencil icon), 'Top 10 FAQs' (with a question mark icon), 'Q&A Chat' (with a speech bubble icon), and 'About' (with an information icon). The main content area has a dark background. At the top right, there is a 'Deploy' button with a vertical ellipsis icon. The main content starts with the title 'UVM Sequences' in white, followed by a large white heading 'Introduction'. Below the heading is a paragraph of white text: 'UVM (Universal Verification Methodology) sequences are a pivotal aspect of transaction-level stimulus generation used in verification environments. They provide an object-oriented approach to creating and managing test scenarios, allowing for efficient, flexible, and reusable stimulus generation. UVM sequences are designed to promote abstraction, enabling test writers to generate complex tests without being tightly coupled to specific testbench components.' Below the paragraph is another large white heading 'Main Points'. Underneath, there is a single numbered list item: '1. **Sequence Execution:** Sequences are initiated using the `uvm_sequence start()` method, which links them to a sequencer.'

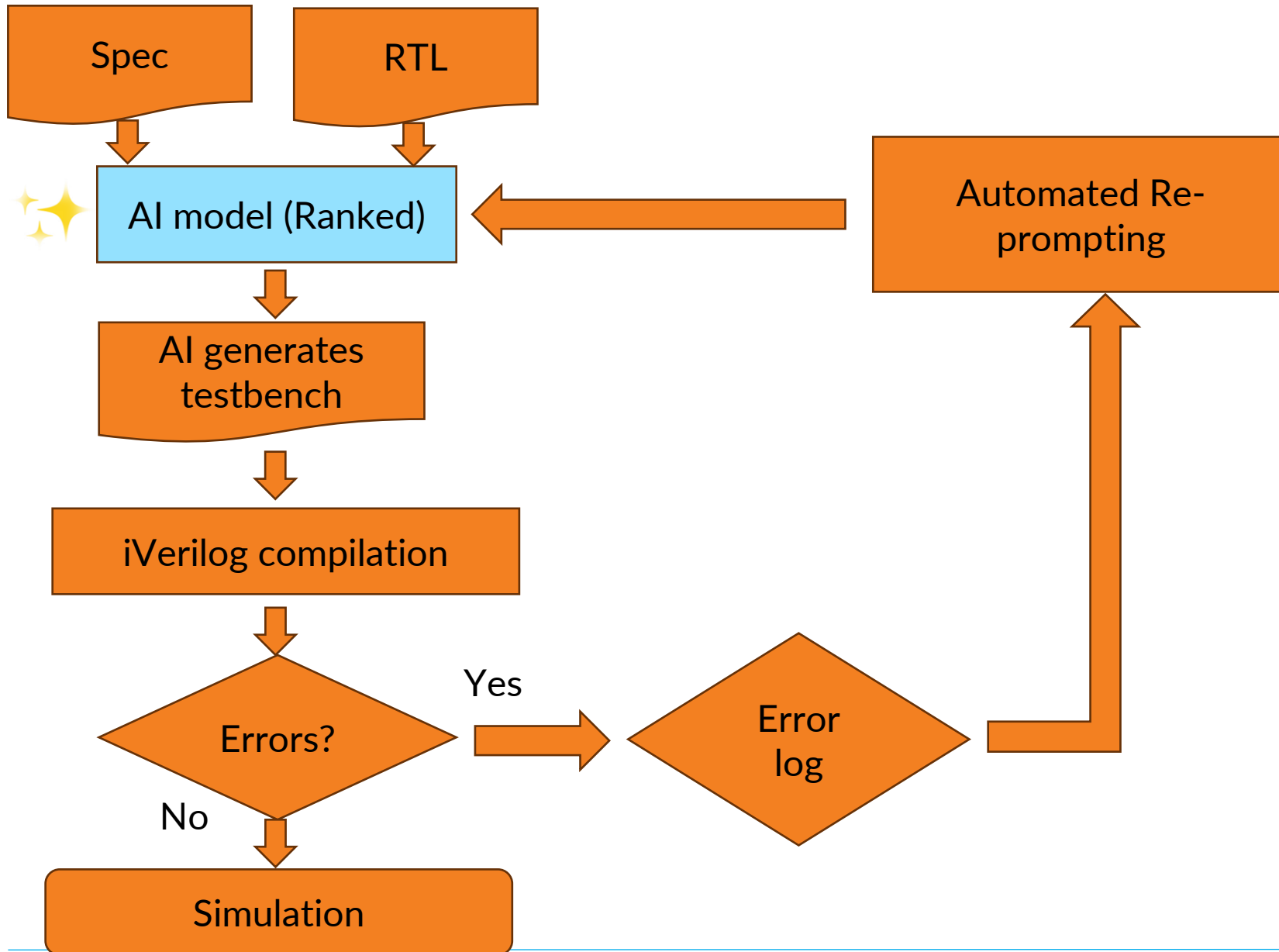
1: UVM AI Training Tool



2: Simple TB Generation – Independent Verification for Designers

- There is always a need for designers to have a basic test bench to make sure the RTL is basically functional before handing it to verification.
- But there is a concern for independence otherwise designers are just verifying their understanding – a single point of failure.
- We demonstrate our tooling that can generate simple test bench from the specification either in Verilog or SV
 - if preferred by the designer
 - or basic UVM if they prefer
- Designers can add “designer knowledge” to their generated test bench
 - For example:
 - Assertions
 - functional coverage
 - A scoreboard function (test bench hooks can be given for that)
 - Verification engineers can decide if they want to reuse them
 - With full knowledge of any associated risks

2: Simple TB Generation Tool




2: Simple TB Generation Tool

About

Tessolve Unit TB Generation & Simulation Tool is designed to automate the creation and refinement of Verilog testbenches.

This application simplifies and accelerates the process of generating and debugging testbenches, providing you with multiple iterations.

New Design 

Edit Testbench Code

Edit Testbench Code

```
`timescale 1ns/1ps
module LFSR_8bit_tb;
reg clk;
reg rst_n;
wire [7:0] Q;

LFSR_8bit uut (
    .clk(clk),
    .rst_n(rst_n),
    .Q(Q)
);

initial begin
    $dumpfile("waveform.vcd");
    $dumpvars(0, LFSR_8bit_tb);
end

initial begin
```


 Developed by CoE Team

2: Simple TB Generation Tool


About


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New Design 

Tessolve Unit TB Generation & Simulation Tool


 Upload Module


 Edit Testbench

 **Compilation**

 Simulation

Compilation

Compilation successful! 

****Go to the Simulation tab**** 

 Developed by CoE Team

2: Simple TB Generation Tool

A quick first cut basic SV testbench generation tool to help designers to get easy debug of the RTL.

Features:

- AI TB generation
- Error feedback
- Tool chain Integration for compilation, simulation

Benefits:

- Error handling
- Accelerate designer “smoke test” verification
 - No need to involve DV
- Time saving
- Tool integration saves lot of time
- Opensource tool set

3: Automating Coverage Closure – The Ultimate Objective

Achieving coverage closure in verification is challenging, consuming up to 80% of efforts. Automation in this area remains a formidable challenge. Tessolve leverages AI to automate this process effectively.

Benefits:

- Reduced verification efforts
- Fast opensource simulation
- High efficiency feedback loop
- Complete automation

Python UVM Test Bench Generation:

- Generation of test bench with numerous "knobs and hooks" to configure the constrained random generation.

Intelligent AI agents:

- By intelligent AI agents and employing a suitable loss function, we guide the system towards the coverage goal.

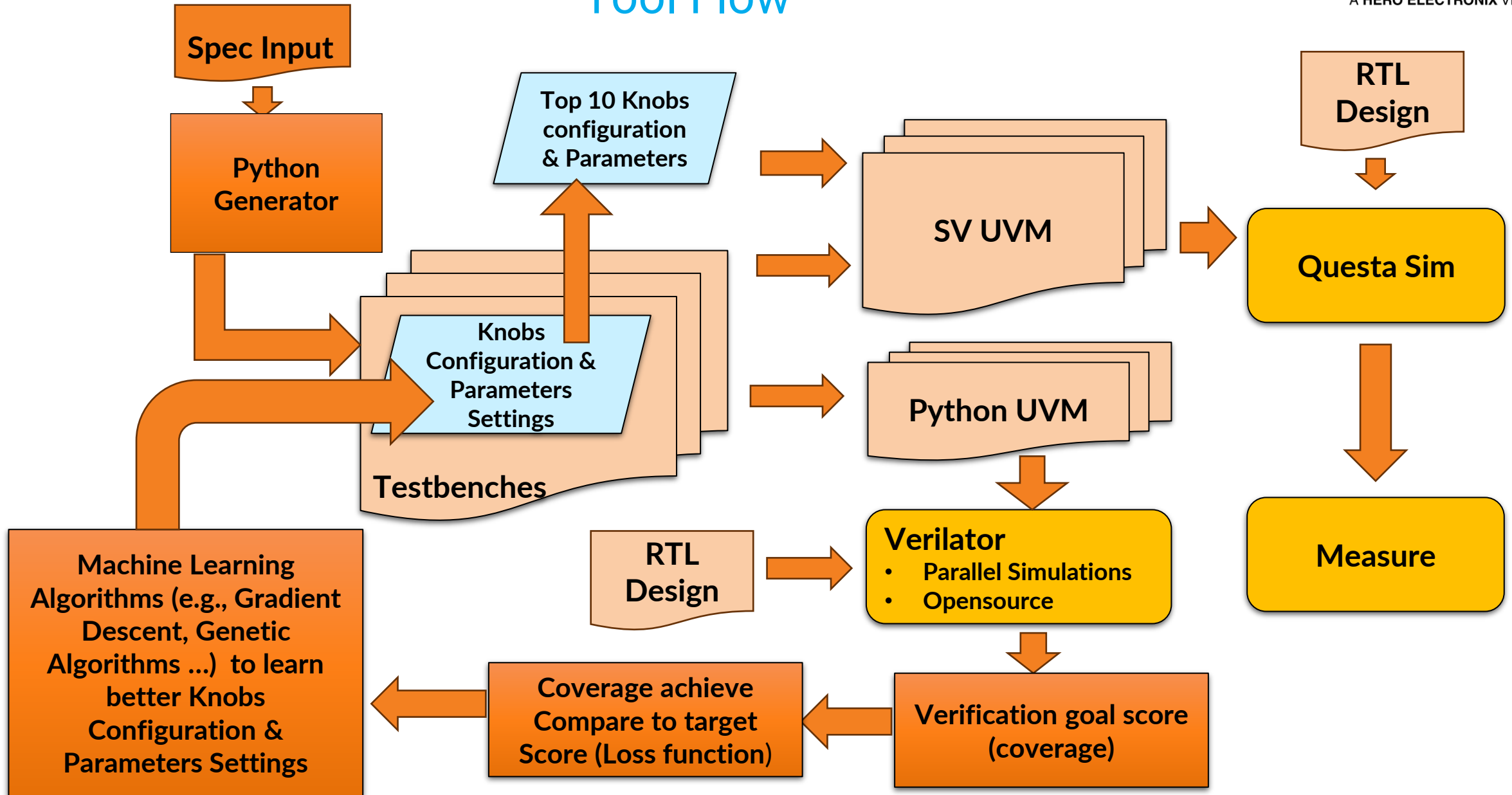
Machine Learning Techniques:

- Techniques such as gradient descent or genetic algorithms are employed by ML to achieve the desired coverage.

Simulation Strategy:

- Multiple simulations are crucial for the ML model to learn effectively. We demonstrate the use of a Python test bench with Verilator for quick, cost-effective simulations before transitioning to System Verilog (SV) with a recognized simulator for signoff. This approach helps mitigate the risk of different randomization outcomes.


Tool Flow




Why Python for TB Generation?

- We can still generate better test benches compared to AI
 - Re-use of previous generation via config files per design
 - E.g. re-use of previous test bench structures such as complex scoreboards
 - Python knows the split between static and dynamic UVM structures
 - Richer set of “knobs, config, and parameters”
 - All collected in a separate file to help the ML learning process
- But under constant review and adding specific AI solutions
 - Add AI for assertion generation
 - And functional coverage generation

Collaboration with DV Flow




Register Extraction




Test Plan Generation



Testcases




Specification Analysis



Coverage Planning



Assertions




Cover points




Testbench Automation




Feature Description



Unit Test Bench Generation

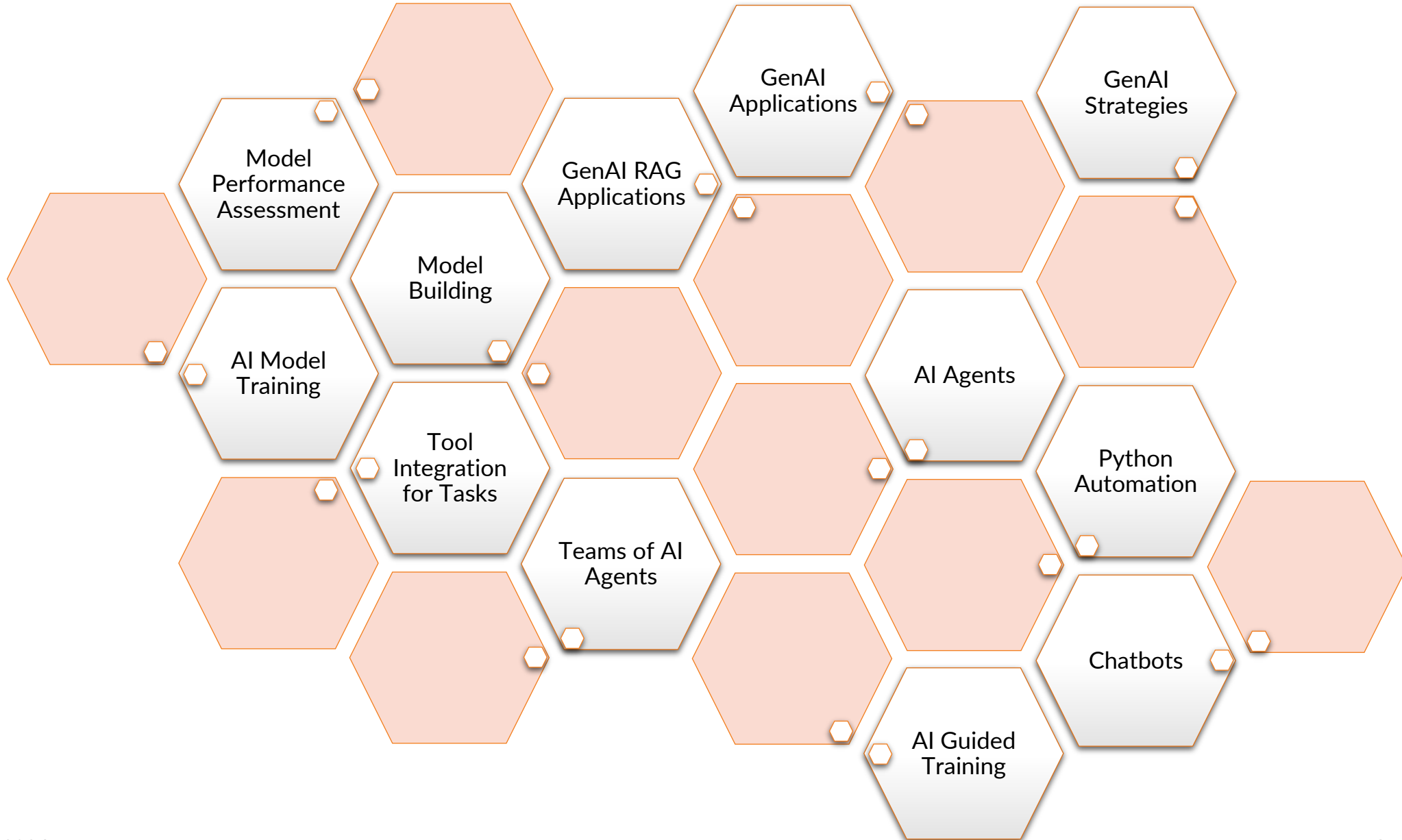


AI Agents for Tasks



Tool Integration & Automated Validation

Collaboration with AI Research



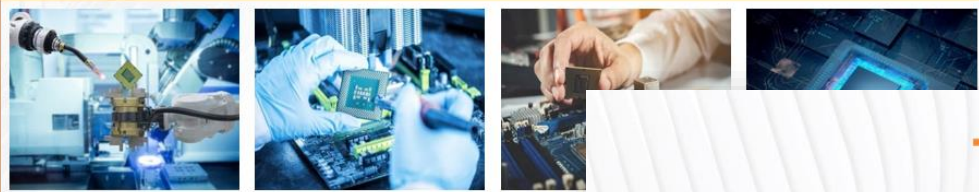
Webinar Series Summary

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Webinar 1: AI Strategy and Eco System for DV

Mike Bartley, SVP, CoE | Marmik Soni, Sr Design Lead, CoE



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Test Engineering

Hardware Design

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Webinar 3: AI Assisted DV Flow & Use cases

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Webinar 2: AI Assisted DV Flow

Mike Bartley, SVP, CoE | Marmik Soni, Sr. Design Lead, CoE



Hardware Design

Embedded Systems

Webinar 1 Registration	
Remote Access	230
Countries	31
Companies	110

Webinar 2 Registration	
Remote Access	216
Countries	35
Companies	105

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THANK YOU



<https://calendly.com/mike-bartley-tessolve/one-one-call>



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