LEVERAGING AMS VERIFICATION AND DMS VERIFICATION FOR EFFICIENCY AND QUALITY IN MIXED-SIGNAL DESIGNS

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AGENDA

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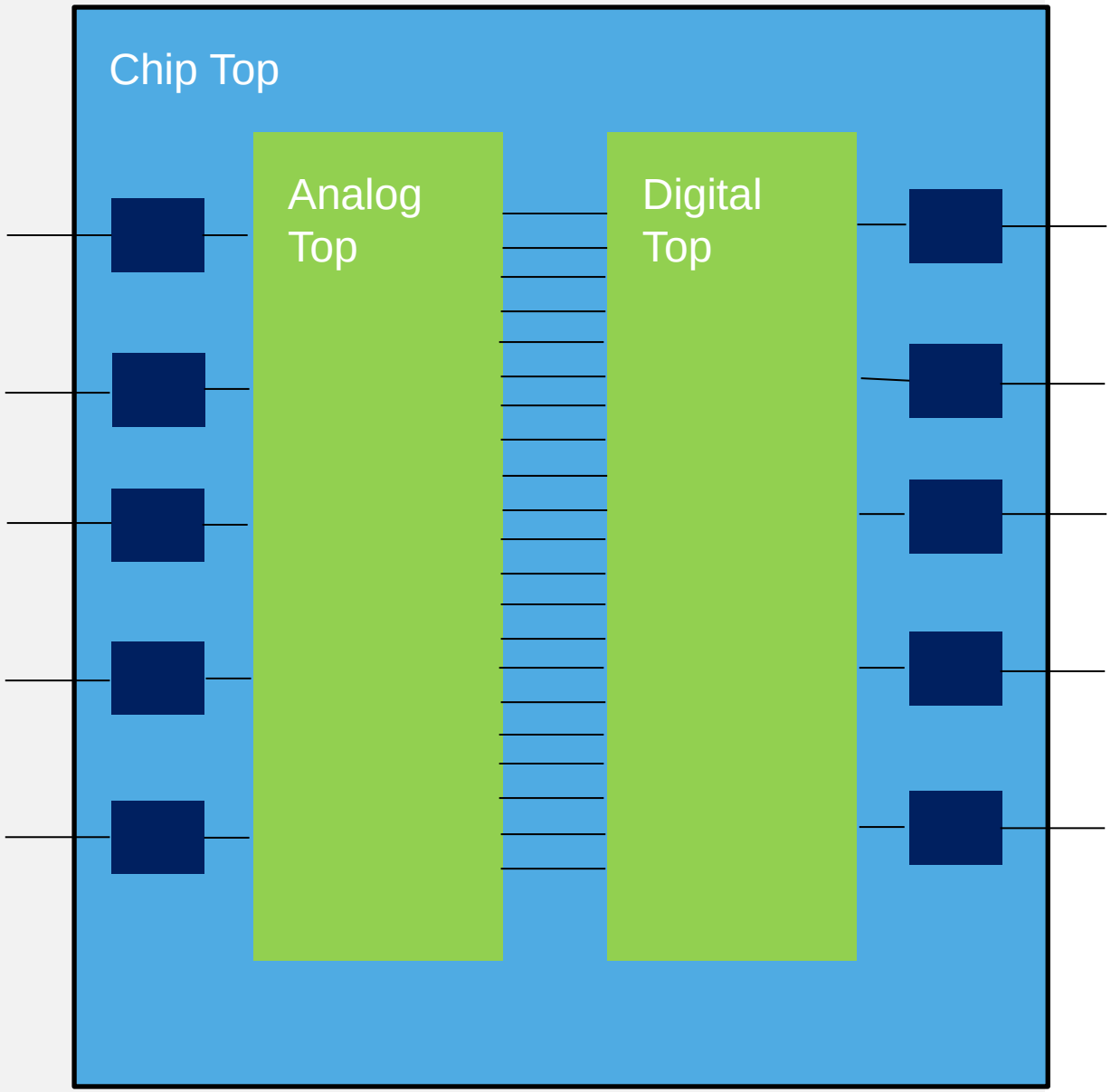


WHAT IS A MIXED-SIGNAL IC

- Mixed-Signal ICs have both Analog and Digital functions together on the chip
- Analog functions are typically implemented using a schematic based design flow
- Digital functions are typically implemented using an RTL-Synthesis-Automated Place and Route (APR) based flow

VERIFICATION OF A MIXED-SIGNAL IC

- Two aspects of Mixed-signal IC verification
  - Verification of electrical parameters, performance, and transient behavior of Analog circuits
  - **Functional verification** at block and **SOC/sub-system level**

- Majority of use-cases involve interaction between Analog and Digital that needs verification at the SOC/sub-system level
  - Most of the digital/SOC level bugs are found here

- Two approaches to SOC/sub-system level verification
  - Analog-Mixed-Signal Verification (AMSV)
  - Digital Verification (DV)

VERIFICATION OF A MIXED-SIGNAL IC

- Analog-Mixed-Signal Verification (AMSV)
  - SOC level verification with Analog focus
  - Analog is typically represented using schematics/models that need the simulator's analog solver
  - Digital is typically represented using behavioral model (Verilog/SV/VHDL etc)
  - A more accurate verification method that is orders of magnitude slower than DMSV
- Digital Verification(DV)
  - SOC level verification with digital focus
  - Analog is typically represented using behavioral models that do not need the simulator's analog solver
  - Digital is typically represented using behavioral model (Verilog/SV/VHDL etc)
  - Orders of magnitude faster than an AMS simulation
  - Accuracy depends on modeling, and model verification

EVOLUTION OF DV INTO DMS

- Evolution of digital verification in Mixed-Signal ICs
  - Digital top only verification
    - Verification of the digital was limited to the digital-top with no true chip level verification
    - Lack of modeling of any analog blocks
    - Analog response is provided by the testbench itself
    - 100% digital only focused verification flow
    - Chip level connectivity and functional coverage are dependent on AMSV
  - Digital top with functionally equivalent models
    - Analog/digital models functionally equivalent to the analog schematics used along with digital top
    - No real netlisting from the actual chip level schematic
    - Still a very digital only focused verification flow
    - Can result in a more accurate digital but chip level connectivity and functional coverage are still dependent on AMSV
  - Digital top with accurate Analog real number models and netlisting from chip level schematics
    - Chip level Digital-Mixed-Signal (DMS) verification
    - More accurate and fast Analog behavioral models are used through Wreal, System Verilog Real Number (SV-RNM), and User Defined Net
    - When combined with robust model verification, can provide reliable SOC level connectivity and functional coverage

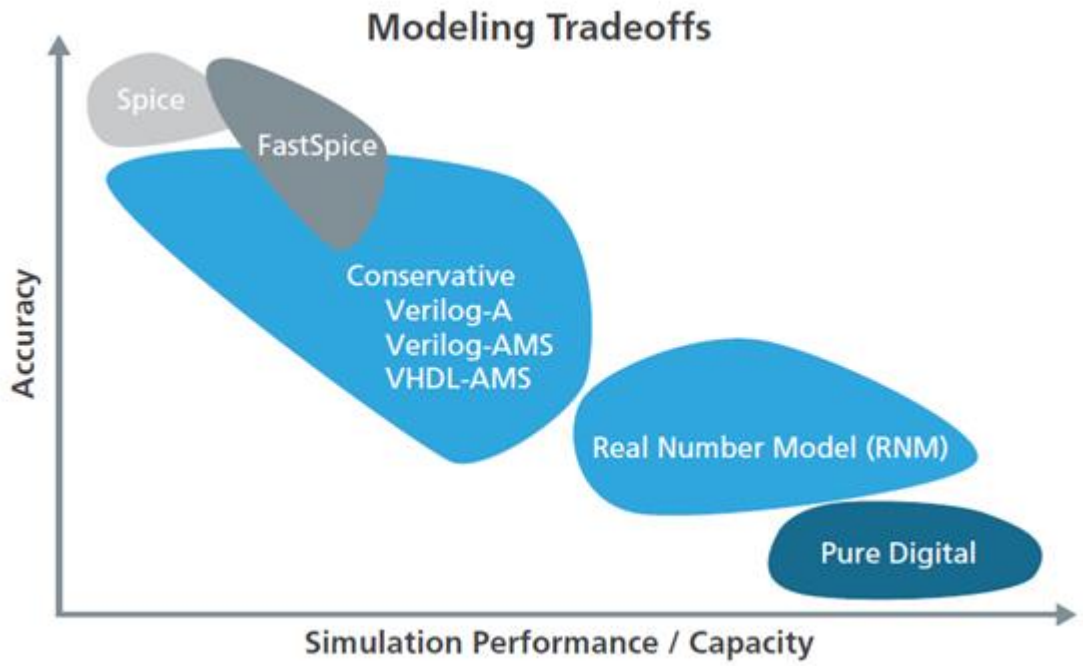
NEED FOR A COMBINED AMS-DMS VERIFICATION FLOW

- AMSV and DMSV flows have the same common goal. They solve the same problem
- With more accurate modeling, Chip level use cases and scenarios previously verified only using AMSV could be verified using DMSV without invoking the analog solver
- Concepts like randomization, coverage etc could be realized at the Chip level leading to a more thorough verification
- Though DMSV could provide a greater share of functional coverage in less time it still cannot completely replace AMSV
- AMSV and DMSV working independently is inefficient, and unnecessarily redundant
- A combined DMS-AMS strategy which leverages on strengths of DMSV, and AMSV flows will reduce cycle times while ensuring quality

A COMBINED AMS-DMS FLOW

- This flow aims to move away from heavy dependence on AMSV for SOC/Chip level verification
- Instead a balanced approach utilizing both AMSV and DMSV is recommended
- Verification Planning
  - Instead of working on separate, and independent Verification Plans, AMSV and DMSV execute a common chip level Functional Verification Plan
  - Verification Plans clearly identify the method to be used to cover each feature – AMSV, DMSV, or Both
  - The classification depends on the following factors-
    - Criticality of the feature – input from product definers, analog designers
    - Maturity of the analog IP and the analog models
    - Existence of a robust analog model Vs schematic verification flow
    - Other factors like analog, and digital design approach, experience of the teams greatly affect the division of verification coverage between AMSV and DMSV.
- AMSV and DMSV leads need to be clear on the limitations and strengths of each flow in verifying each feature

A COMBINED AMS-DMS VERIFICATION FLOW



- Source: Solutions for Mixed-Signal SoC Verification New techniques that are making advanced SoC verification possible By Kishore Karnane and Sathishkumar Balasubramanian, Cadence Design Systems

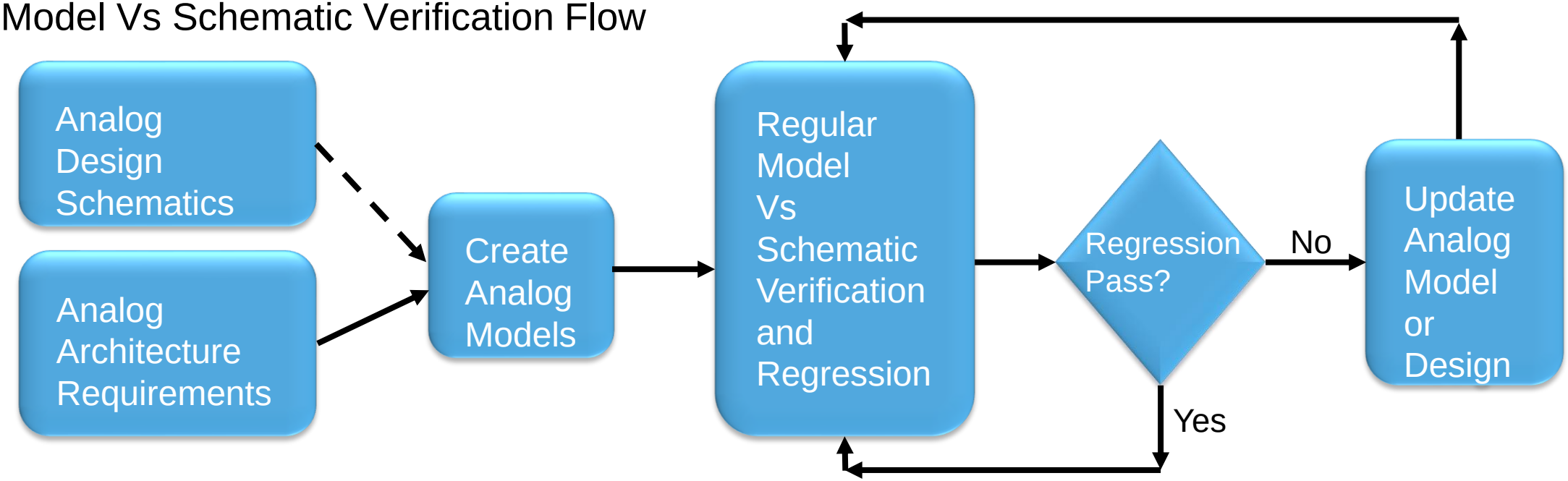
- Figure shows the Accuracy Vs Simulation Performance tradeoff
- DMSV
  - Real Number Model (RNM) or Wreal
- AMSV
  - Spice/FastSpice
  - Verilog-A, Verilog-AMS, VHDL-AMS
- The verification strategy should aim at extracting maximum coverage using DMSV while maintaining needed accuracy
- As teams invest in development of accurate and more sophisticated analog models, coverage share could be transferred from AMSV to DMSV

TRANSITIONING FROM AMS-DV TO AMS-DMS FLOW

- Alignment from other disciplines
  - For successful AMS-DMS flow execution alignment is needed from Analog Design, Digital Design, AMSV, DMSV, and Modeling teams
  - Design teams need to adopt a more Top-Down design approach
    - Define the chip-top level pins, architecture, sub-block ports
    - Define sub-block level, and Analog-Digital interactions clearly before design implementation
    - Well defined partitioning of analog, and digital blocks at chip, and sub-block level
  - A common testbench for AMS and DV is desirable
    - State of the art tools allow for the development of a common TB for AMS and DMS
    - The test bench config view determines if the analog solver is invoked or not in a given sim there by allowing the same test to be run using AMSV or DMSV
    - AMSV tests and checkers could be pipe-cleaned using RNM models before analog schematics are ready
- Modeling and model verification
  - The integrity and reliability of DMSV depends on the availability of accurate and well-written analog models
  - Analog models should be thoroughly verified against schematics
  - The Model Vs Schematic regression should be run whenever the design changes

MORE ON MODELING

- Model Vs Schematic Verification Flow



- Models could be developed by Analog designers, Modeling engineers, or AMSV engineers
- With a top-down design approach, analog models could facilitate early proof of concept of the chip architecture even before any design effort has actually begun
- Analog models could supplement design architecture definition
- Analog IP development requirements could be extended to include analog models for each IP

COMBINED AMS-DMS FLOW – SOME PIT FALLS

Case 1 – An AMSV heavy approach with very simple analog models

- Given the longer simulation times for AMSV, this approach results in very large verification cycle times
- AMSV effort becomes the bottleneck for tapeout

Case 2 – A DMSV heavy approach with very complex analog models

- In this approach even minute features like analog trims are modeled
- Given the iterative nature of analog design, this needed the models to be updated too often
- DMSV effort becomes the bottleneck as model failures delay regression closure

Case 3 – An AMSV-DMSV flow without a strong top-down design flow

- Without a strong top-down design flow, analog schematics, sub-block ports, and the analog-digital interface change frequently requiring frequent netlist, and testbench debug
- DMSV team spends a lot of time in re-netlisting the design, and in testbench debug

CONCLUSIONS

- A combined approach for SOC level functional verification of Mixed-signal designs has been presented
- Adopting a well balanced, and combined AMS-DMS verification flow is expected to reduce total time and resources spent on verification
- Having a robust analog model creation, and verification flow will ensure reliability in the coverage achieved through DMS
- Some pit falls in the suggested approach also have been presented based on some real case studies