TESSOLVE

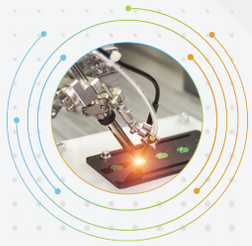
VLSI Design

VLSI Chip Design and Engineering Services

Tessolve's VLSI team of nearly 900 engineers provides specs-to-GDSII solutions to our customers. Together with Tessolve's post-silicon engineering solutions, we provide end-to-end ASIC development services, enabling our customers to realize successful silicon.

VLSI Design /Technology Services Overview

- VLSI Chip Design Solutions from "Specifications to GDSII signoff" for Analog, Digital, and Mixed Signal chips across process nodes from 350nm down to advanced 3nm nodes.
- Digital Design Turnkey Capabilities – Architecture, RTL Design, Verification, DFT, Synthesis & STA, Physical design till GDSII signoff.
- Analog/AMS Design Turnkey Capabilities – Architecture, Circuit Design, Analog Modelling, Layout Design, AMS Verification.
- Robust Technical Program Management and Quality Processes to ensure first pass Silicon.
- In-house EDA tool licenses and management of Cloud compute infrastructure for turnkey program execution.



Our IC Capability

- Analog & Mixed Signal
- RTL Design
- Design Verification (DV)
- Design for Test (DFT)
- Physical Design
- FPGA Emulation & Validation

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Analog & Mixed Signal (AMS) Design

The Analog and Mixed-signal design team at Tessolve specializes in High-quality design for different applications with process nodes varying from 350 nm to most advanced 3nm designs. The IPs were developed for various industry verticals like Automotive, Communication, Consumer, Medical, IoT, etc. The competent team has rich experience in delivering more than 70+ silicon-proven Analog chips during the last few years with full ownership of the delivery from Spec to GDSII signoff, supported with silicon validation to global semiconductor companies.

- Complete Analog Design life cycle from specs to post-silicon validation
- Expertise in developing Full IP & Block level
- Expertise in CMOS/FinFET process nodes: 3nm, 5nm, 7nm, 10nm, 14nm, 22nm, 45nm, 65nm, 90nm, 130nm, 180nm & 350nm

RTL Design

Tessolve offers RTL design services from product specifications for both IP and SOC Development. Offerings include:

- Standard and Complex IP Block Design and Development
- SoC and Sub-system Integration, Clock and Reset design, Clock gating, Low-power design, UPF definition
- RTL Quality Checks: Lint, CDC, Automated property checks, Low-power checks
- Protocol Experience: HSIO Protocols (PCIe, USB, MIPI), AMBA protocols (AXI/AHB/APB), Memory interfaces (DDRx/LPDDRx), Low-speed peripheral interfaces (I2C, SPI, UART, MDIO, I2S)

Design Verification

Verification is one of the most significant tasks in silicon development and has the most significant impact on the critical business drivers of quality, schedule, and cost. With its large pool of verification resources and investments in tools and verification methodologies, the customer is in safe hands to get all its validation needs to be addressed with Tessolve.

- IP and SOC-level Verification using C/C++, SV-UVM methodologies
- CPU (ARM, RISC-V, Tensilica) processed based on Verification
- Robust Verification planning to achieve Functional and Code Coverage goals
- Power-aware verification
- Gate-level simulations and regression management
- Tools for verification productivity – Formal Verification, PSS

Design For Test

Our team of Design for Testability experts can help with the chip DFT architecture and implementation to increase IC test coverage, yields, and quality. Coupled with our large ATE test team and infrastructure, we are uniquely placed to build a coherent strategy and implement DFT that improves the testability of the IC in the post-silicon phase for first-pass silicon. Tessolve's DFT service offerings include the following:

- DFT architecture and scan methodology
- RTL-level DFT quality checks
- Scan insertion, ATPG pattern generation, and Verification
- Memory BIST and Boundary Scan
- Fault Coverage Analysis, Debug, and Improvement
- Post-silicon debug support

Physical Design

Physical design is a process in the VLSI system in which the structural netlist is transferred from the front-end design to the back-end design team for transforming into a physical layout database that contains geometrical design information for every physical layer and is used for interconnections. Tessolve's physical implementation services include:

- Physical design for multiple foundries and advanced Process nodes down to 5nm
- Constraints planning, Synthesis, and Static Timing Analysis
- Digital and Mixed-signal Full-chip integration
- ARM and RISC-V processor-based designs and GPU designs
- Low-power designs
- Block-level and Full-chip level implementations targeted to consumer, mobile, industrial, gaming and data center applications
- Tape-out signoff checks for GDS release to the foundry

FPGA Prototyping

- Experience with the Xilinx & Intel FPGA device family
- FPGA-based emulation, FPGA partitioning, ASIC to FPGA & FPGA to ASIC conversion
- Custom board development and FPGA validation

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